SWITCHING AND REDUCTION OF COMMON MODE VOLTAGE OF MULTILEVEL-H-CASCADED CONVERTER FOR MEDIUM VOLTAGES

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Abstract:

This paper presents reduction of common mode voltage in a multilevel H-cascaded converter for medium voltages. It is well known that a conventional two-level pulse width modulated (PWM) converter generates high frequency common mode voltage with high dv/dt. In the same way, commonly used multilevel converter modulation schemes generate common mode voltage. Multilevel voltage source converters are getting increased importance for applications in the medium and high voltage range. Due to the easy construction of H-cascaded converter, it can play an important role in the industry. Common mode voltage may cause motor shaft voltages, bearing currents and electromagnetic interference (EMI). The common mode voltage depends on the switching method and earth mass. In order to reduce the common mode voltage, a suitable filter has been used and common mode voltage has been reduced to zero. Sinusoidal (sine-triangle) PWM scheme is being used for this purpose and simulation results are being presented in this paper by using software "Simplorer".

Key words: cascaded converter, common mode voltage, motor shaft voltage, bearing current, electromagnetic interference (EMI)

I INTRODUCTION

The importance of advanced power electronic systems is increasing due to the trend of decentralised power generation and the deregulation of energy markets. Several types of multilevel converters have been investigated for these new applications [1-6]. The basic requirements for this application field are high voltage and high power. Besides this, many other aspects, regarding to the industrial implementation of these converters, have to be taken into consideration. A particular advantage of this topology is that the modulation, control and modulation requirements of each bridge are modular [7]. However, each single phase inverter has its own supply. Multilevel inverter structures have been developed to overcome the shortcomings in solid state switching device ratings so that they can be applied to high voltage electrical systems. There have been a number of mitigation techniques suggested for the bearing current and conducted EMI. However, few of them have addressed the common mode voltage successfully and directly none of them have been found within the context of multilevel PWM inverters.

At sinusoidal supply voltages, bearing currents may flow in a closed loop comprising the shaft, both end-shields and the housing. These circulating currents are caused by magnetic asymmetries of the stator yoke, which result in a ring flux in the yoke inducing the so-called shaft voltage in the loop. Up to a certain value of the shaft voltage the circulating current is zero; however, at higher shaft voltages the circulating currents destroy the bearing within a short period of time. In many cases the shaft voltage can be limited to uncritical values by optimisation of the yoke geometry; otherwise the insulation of one bearing is a common measure of protection. Novel effects occur at supply by modern voltage source converters (VSC), caused by capacitive coupled bearing voltages, which initiate the so-called EDM-currents (Electric Discharge Machining) through one motor bearing, and by shaft voltages of high frequency. This effects result from the common mode voltage of the inverter which represents a zero sequence component of the voltages and which is inherent to all control schemes of PWM inverters. In [8] , a dual bridge inverter (DBI) is presented to generate zero common mode voltage. For this work many filters, described in [9-10], have been researched to reduce the common mode voltage. With the help of a filter (fig. 13), the common mode voltage has been reduced to zero (fig. 14). All simulation results are being presented in this paper.

II STRUCTURE AND OPERTATION OF H-CASCADED BRIDGES

A cascaded multilevel inverter (fig. 1b) consists of H-bridge (single-phase full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources. Fig. 1a shows a rectifier with separate supply sources. Each inverter level can generate three different output phase voltages, $+V_{dc}$, 0 and $-V_{dc}$ by connecting the dc sources to the ac output side by different combination of four switches S_1, S_2, S_3 und S_4. The phase voltage depends on the number of levels. With enough levels, using this fundamental switching technique results in an output voltage of the inverter that is almost sinusoidal. From fig. 1b it is clear to see that there are four possible switching states of a single phase converter, which are stated in fig. 2a-d. To obtain the dc-bus voltage $-V_{dc}$, switches S_1 and S_4 are turned on simultaneously. Turning on switches S_2 and S_3 yields V_{dc}. By turning on S_1 and S_3 or S_2 and S_4, the output voltage is 0. The fundamental frequency for this circuit is 50Hz, while the switching frequency is 3kHz.. Electromotive Force (EMF) e can be

calculated from equation (2), which for this work has been taken 3.81kV and output RMS-current (Root Mean Square) is selected 1.2kA.

The voltages v_1, v_2, v_3 and v_{12} in fig. 1b of three inverters are being described in equation (1):

$v_1 = v_2 = v_3 = V_{dc}$ and

$v_{12} = v_2 - v_1 = 2V_{dc}$ (1) $e = MV_{dc}\cos(\omega t+\varphi)$ (2)

In equation (2) is M = 1; and V_{dc},= 3.81kV.

Abbreviations and symbols:

M = Modulation index; and V_{dc},= dc-bus voltage, fig. = figure; equ. = equation; L_L = Last inductor; L_F = Filter inductor; C = Condensor; C_F = Filter condensor

III DESCRIPTION AND SIMULATION

Typically, two kinds of bearing currents are caused by the bearing voltage which pass only one bearing of the motor and flow back to the converter. The so-called du/dt-currents through the capactor of the bearing are less than maximal several hundred mA and therefore they cannot destroy the bearings. By contrast, the EDM-currents, stochastically occurring break downs of the grease film at high peak values of the bearing voltage, are of great practical importance. The endangering factors are the peak values of the EDM-currents and its repetition rate. The repetition rate grows with the switching frequency. The common mode voltage causes common mode currents. It depends on the kind of grounding system whether these zero sequence components of the currents penetrate the active parts of the motor. Statistics of bearing faults show that many bearing deficiencies at converter supply are caused by poor grounding for frequencies in the kHz range. The common mode currents penetrating the stator winding don't cause a linear voltage drop along the length of the winding conductors, because they flow partly through the capactor between winding and core. Consequently the currents in the two leads of each turn are not yet identical. The impulse shaped shaft voltage obviously acts as initiator for the circulating currents, the emf of which is the shaft voltage of basic frequency. This relationship was unknown up to now [11]. The power circuit of a three phase and three level inverter is shown in fig. 1b. Assuming that of the two power switches in each leg of the inverter one and only one is always on, that is, by neglecting the time intervals when both the switches are off (blanking time), three switching variable phases a, b, and c can be assigned to the inverter. It is easy to show that the instantaneous line to line output voltages, as described in equ. (3), v_{12}, v_{23} and v_{31} are given by:

$$\begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \end{bmatrix} = V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3) \qquad \begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (4)$$

In a balanced three phase system, the instantaneous line to neutral output phase voltages, v_{An}, v_{Bn} and v_{Cn} has been expressed in equ. (4), where a, b and c are the phase legs in equation (3) and (4).

Equation (3) and (4) allow easy determination of the line to line and line to neutral output voltages for all states of the converter. The line to line voltages can assume five values ($\pm 2V_{dc,}$ $\pm V_{dc}$ and 0), while the line to neutral voltages assume only three values ($\pm V_{dc}$ and 0) as shown in fig. 4 and 5.

For a given input phase voltage v_s (also called line to neutral voltage) of 2,2kV for a single converter (fig. 1a), the dc-bus voltage has been calculated as given in equation (5) and shown in fig. 3b:

$$V_{dc} = \sqrt{3} * \hat{v}_s = \sqrt{3} * 2.2kV = 3.81kV \tag{5}$$

In equation (5) $\hat{v}_s$ is the peak value of input phase voltage. In equations (3-5) it has been assumed that dc-bus voltage is, $v_{dc} = V_{dc}$ = constant. But it is not quite correct because the simulation results have shown that v_{dc} is the sum of voltages [12], as described in equation (6):

$$v_{dc} = V_{dc} + \sum_{i=1}^{\infty} \hat{v}_{dc,i} \sin(\omega_{dc,i} t + \varphi_{dc,i}) \tag{6}$$

The reason for equation (6) is that as soon as the switches are being switched on, the dc-current takes a part of pulses and this part of pulses produces the ripples. Therefor the dc-bus voltage shows sine waves. The lowest frequency of a dc-bus voltage should be twice (100Hz) of a single phase (fig. 3b) and 6 times (300Hz) of a three phase converter than that of basic frequency [12]. The amplitude of the input line to line voltage of one inverter is also equal to $\sqrt{3} * v_s$. The maximum amplitude of a dc-bus voltage v_{dc} should be $2.34 * v_s$ [13]. The output line to line voltages v_{12}, v_{23} and v_{31} (fig. 1b) have the maximum amplitude of $2v_{dc}$, whose simulation results are described in fig. 4. The maximum amplitude of output phase voltages (fig.5) v_{An}, v_{Bn} and v_{Cn} is 1/2 of the output line to line voltages. The common mode voltage (v_{cm}) is however 1/3 of the line to line voltages. The simulation results of output phase voltages and common mode voltage can be seen in fig. 5 and 7. By applying the Kirchhof's law of voltages (KLV) $\sum v = 0$ for the loops from fig. 1b, described in equ. (7) and (8), the line to line voltage v_{12} is equal to:

$v_{12} + v_1 - v_2 = 0 \Rightarrow v_{12} = v_2 - v_1$ (7) and $v_{12} + v_{Bn} - v_{An} = 0 \Rightarrow v_{12} = v_{An} - v_{Bn}$ (8)

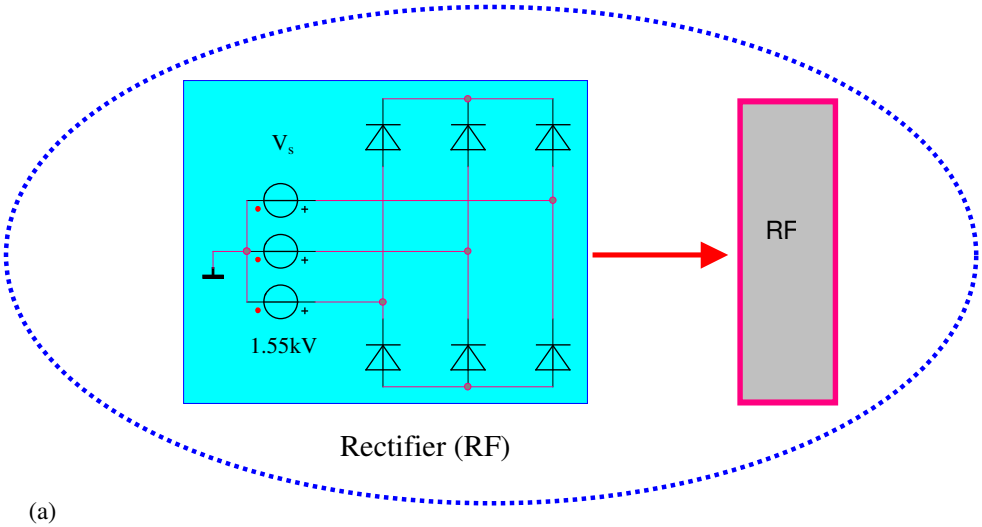
From fig. 1b it is to see that the sum of the output phase voltages ($v_{An} + v_{Bn} + v_{Cn} = 0$) is equal to zero, which can be verified from fig. 6. Similarly, the sum of the output phase currents ($i_{An} + i_{Bn} + i_{Cn} = 0$) is equal to zero. The fig. 12 and 8 show the output phase currents with and without filter. With the help of a filter and earth mass (fig. 9), the harmonics of common mode voltage has been reduced (fig.11) but the amplitude remains constant. The mathematical description for reduction of common mode voltage (fig. 14) according to fig. 13 has been given in the following equations (9-13). The fig. 10 shows the voltages on the filter capactors. By using the law of voltages ($\Sigma v = 0$) for fig. 13 the equations (9-11) have been achieved for common mode voltage.

$v_{cm} = v_{CF1} - v_{L1} - e_u$ (9) $v_{cm} = v_{CF2} - v_{L2} - e_v$ (10) and $v_{cm} = v_{CF3} - v_{L3} - e_w$ (11)

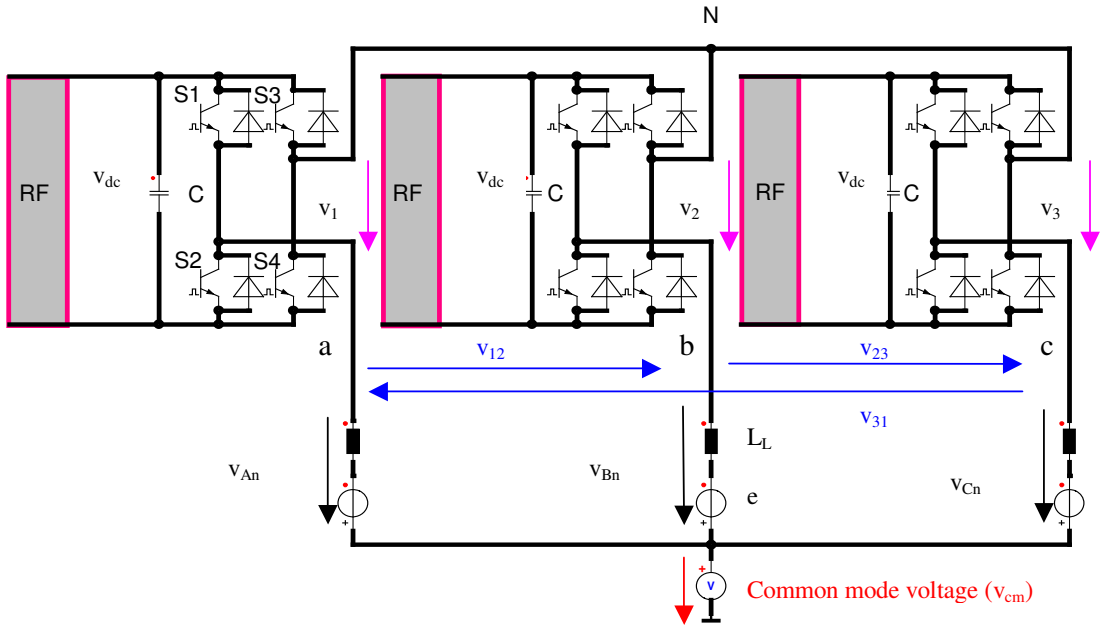
By adding the equations (9-11) :

$$v_{cm} = \frac{1}{3}[v_{CF1} + v_{CF2} + v_{CF3} - (v_{L1} + v_{L2} + v_{L3}) - (e_u + e_v + e_w)] \tag{12}$$ and $$v_{cm} = 0 \tag{13}$$

In equation (12) the electromotive forces e_u, e_v and e_w are free from common mode voltage and therefore the sum of e_u, e_v and e_w is zero. As the last is symmetric in fig. 13, it makes a symmetric system and therefore the sum of the voltages ($v_{CF1} + v_{CF2} + v_{CF3} = 0$, $v_{L1} + v_{L2} + v_{L3} = 0$) is zero and the common mode voltage v_{cm} between the point n and 0 is zero. The equ. 13 and fig. 14 show that the common mode voltage is zero.



(a)



Parameters: V_s = 1.55kV, f_1 = 50Hz, f_s = 3kHz, M = 1, e = 3.81kV, C = 2.46mF, L_L =7.14mH

(b)

Fig 1: (a) Rectifier (b) Three phase and three level H-cascaded multilevel converter

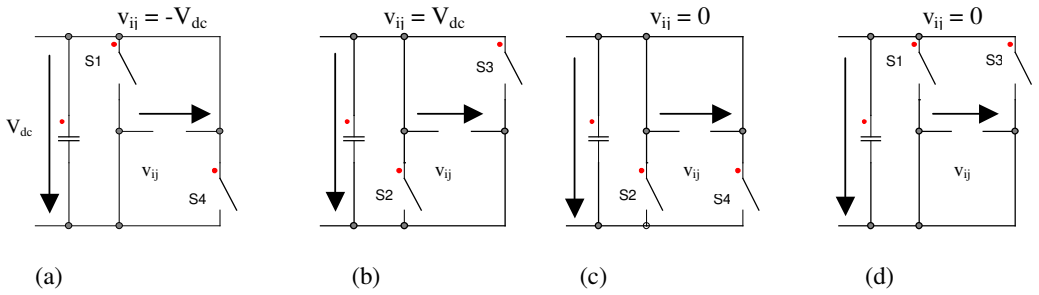


Fig. 2: Four possible switching state (a-d)

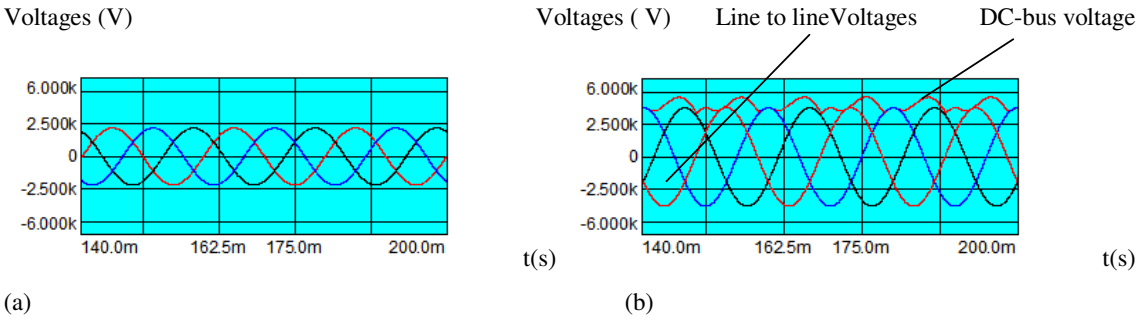


Fig. 3: Input (a) phase voltages (b) line to line voltages and dc bus voltage of a single phase converter

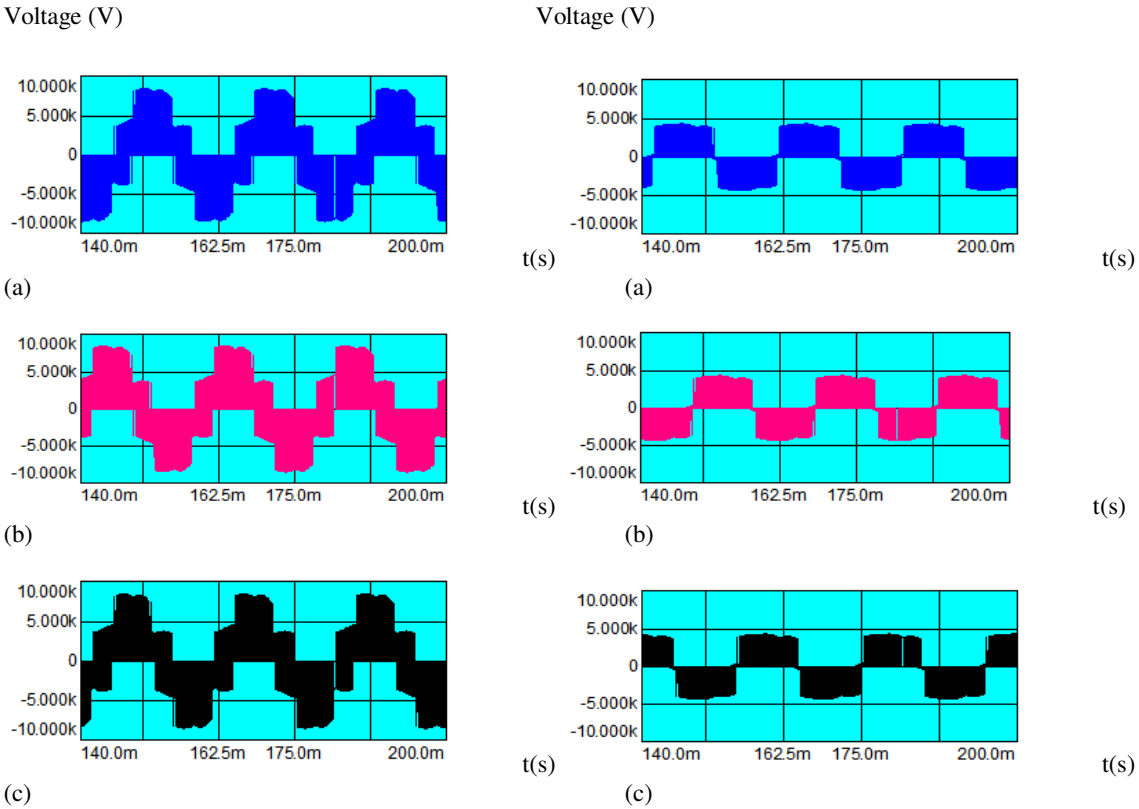


Fig. 4: Output line to line voltages (a) v_{12} (b) v_{23} (c) v_{31}

Fig. 5: Output phase voltages (a) v_{An} (b) v_{Bn} (c) v_{Cn}

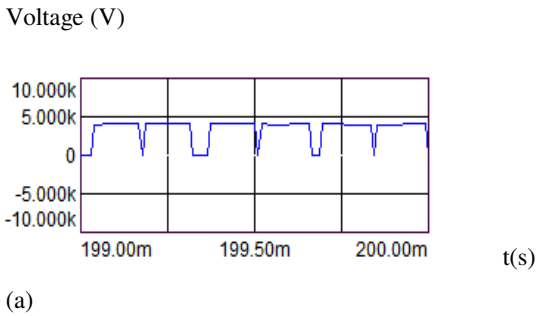


Fig.6: Phase Voltages (a) v_{An} (b) v_{Bn} (c) v_{Cn}

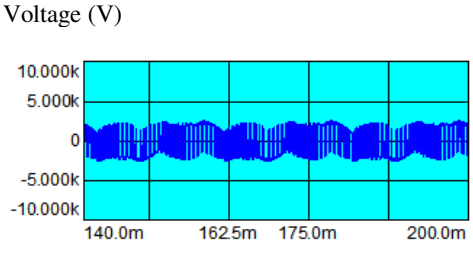


Fig. 7: common mode voltage without filter

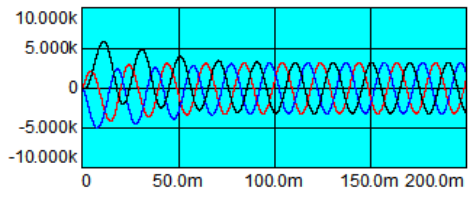


Fig. 8: Output phase currents (i_{An}, i_{Bn}, i_{Cn}) without filter according to fig. 1b

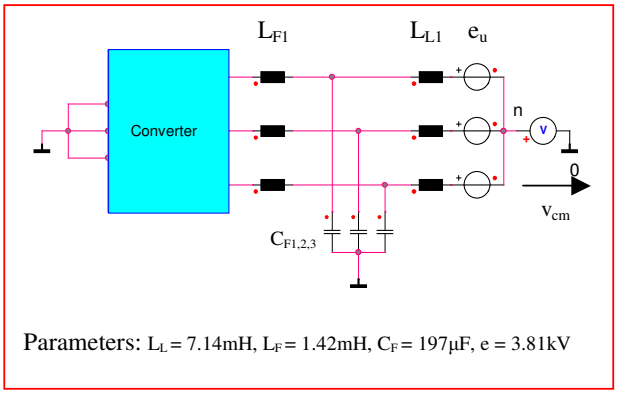


Fig. 9: Circuit of H-cascaded converter with filter and earth mass

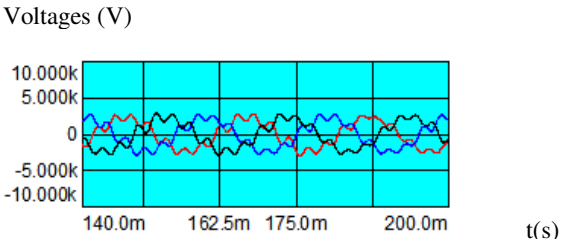


Fig. 10: Voltages on the condensors (C_F)

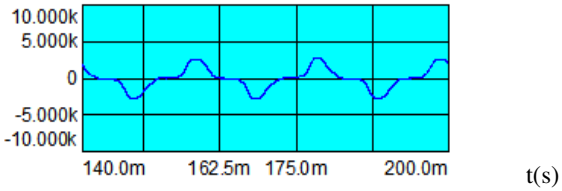


Fig. 11: Common mode voltage with Filter and earth mass according to fig. 9

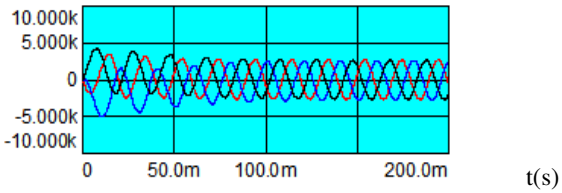


Fig. 12: Output phase currents (i_{An}, i_{Bn}, i_{Cn}) according to fig. 9

In fig. 7 and 11 the common mode voltage has been explained according to the circuits from fig. 1 and 9. By comparing these common mode voltages it can be seen that although throug a filter and earth mass (fig. 9) the

harmonics have been reduced but the amplitude remains the constant. In order to reduce the amplitude of common mode voltage the following circuit (fig. 13), with a filter connected with neutral ponit n and zero point 0, has been used and mathematical description has been given in equations 9-13).

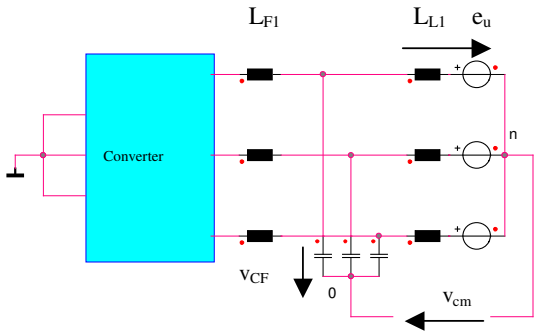


Fig. 13: Circuit of H-cascaded converter with filter

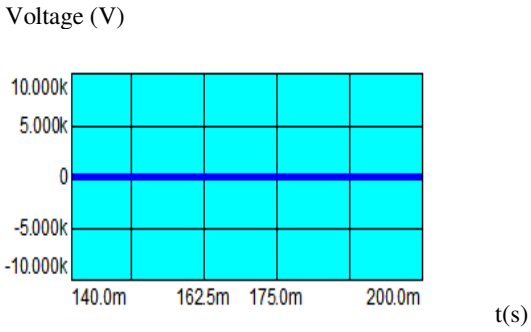


Fig. 14: Common mode voltage according to fig. 13

Advantages of H-cascaded converter

Multilevel H-cascaded converter can overcome many problems i.e. dielectric stress and voltage harmonics. Due to the following advantages, the multilevel H-converter can play an important role in the industry.

1. As H-converter based on two level inverter, the topology is very simple.
2. No additional diodes and capacitors are needed, as for other multilevel converters, i.e. neutral point clamped and flying capacitors inverters.
3. Voltage can be equally divided on all elements. Die structure can be extended up to 2s+1 levels. Die harmonics can be reduced by increasing the no. of levels.

IV Discussion and Conclusion

The H-converter circuit under consideration provide high power drives at medium to high voltage levels, using IGBT technology. The H-bridge circuit has been exploited as a commercial product [6]. Switching methods, filters and earth masses influence the common mode voltage. With a proper switching methode, a suitable filter and choosing the zero ponit in the circuit the harmonics and common mode voltage can be reduced. The common mode voltage depends on switching method and earth mass. The research has been made by using many kinds of filters and earth masses and also modifying the circuit. With the help of a filter and finding the zero point in the circuit the common mode voltage has been reduced to zero.

References:

[1] Nabae, A.; Takahashi, I.; Akagi, H.: “A new neutral-point clamped PWM inverter” IEEE Trans. Ind. Application, vol. IA-17, pp. 518-523, Sep/Oct. 1981.

[2] Yuan, Xiaoming; Barbi, Ivo: “A new diode clamping multilevel converter” IEEE Trans. Ind. Application, vol. 15, pp. 495-501, March 1999.

[3] T.A. Meynard; H. Foch: “Multilevel choopers for high voltage applications”, EPE. Drives Journal, vol. 2, no. 1, p. 41, March 1992.

[4] C. Hochgraf; R. Lasseter; D. Divan; T.A. Lipo: “Comparision of multilevel inverter for static var compensation”, in Conf. Rec. IEEE-IAS Annu. Meeting pp. 921-928, Oct. 1994.

[5] Peng, F.Z.; Lai, J.S.: “Multilevel cascade voltage source inverter with separate DC sources”, U.S. Patent 5 642 275, July 1997.

[6] P. Hammond: “A new approach to enhance power quality for medium voltage ac drives”, IEEE Trans. Ind. Appl., vol. 33, pp. 202-208, Jan/Feb. 1997

[7] M. Marchesoni; M. Mazzuchelli; and S. Tenconi: “A non conventional power converter for plasma stabilisation”, in Proc. IEEE PESC 88, 1988, pp 122-129.

[8] A. von Juanne; H. Zhang: “A dual- bridge inverter approach to eliminating common mode voltages and bearing and leakage currents”, IEEE Trans. Power Elec., vol. 14, pp. 43-48, Jan. 1999.

[9] M. D. Manjrekar; T. A. Lipo: Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Engineering drive, Madison, WI 53706 USA., “An Auxiliary Zero State Synthesizer to Reduce Common Mode Voltage in Three Phase Inverter”, 1999.

[10] N. Hanigovszki, J. Poulsen and F. Blaabjerg, Members IEEE; “A novel output filter topology to reduce motor overvoltage” Trans. Ind. Application IEEE, vol. 40 no. 3, May/June 2004.

[11] A. Mertins, B. Ponick; “Untersuchung und Berechnung von elektrischen Maschinen und Antriebssystemen” Institute of drive system & power electronics, Hannover university- Germany, 11 May. 2005.

[12] F. Jenni, D. Wüest; “Steuerverfahren für selbstgeführte Stromrichter” Hochschulverlag AG an der ETH Zürich, B.G. Tubner Stuttgart, Germany 1995.

[13] K. Heumann: “Grundlagen der Leistungselektronik“, B.G. Teubner Stuttgart, Germany 1996.