HARMONIC REDUCTION FOR THREE PHASE VOLTAGE SOURCE INVERTERS

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ABSTRACT: Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are the most popular modulation strategies for Multi level inverters. Two level inverters is the basic technique to implement any level. It becomes difficult in high voltage & high power applications due to the increased switching losses and limited rating of the dc link voltage. Multilevel inverters are used in high voltage and high power applications with less harmonic contents. This paper proposes a theoretical analysis and software implementation for two level SVPWM & three level SVPWM inverters and three-level SPWM inverters. This software implementation is performed by using MATLAB/SIMULINK software. This paper gives comparison between two level & three level inverters using SVPWM technique. Also this paper gives comparison between three level inverters using SVPWM and SPWM technique. The simulation study reveals that three-level SVPWM inverter generates less THD compared to two-level SVPWM inverters & Three-level SPWM inverters.

Key words—SVPWM, SPWM, THD, TWO &THREE LEVEL INVERTERS

1. INTRODUCTION

In Sinusoidal Pulse width modulation (SPWM) we generate the gating signals by comparing sinusoidal reference signal with a triangular carrier wave. SVPWM (Space vector pulse width modulation) technique was originally developed as a vector approach to PWM for three phase inverters. It is an advanced computation method and it is quite different from reaming methods. The Space Vector PWM of a three level inverter provides the additional advantage of superior harmonic quality. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly [6]. As the number of levels is increased, the amount of switching devices and other component are also increased, making the inverter becoming more complex and costly.

In case of the conventional two level inverter configurations, the harmonic reduction of an inverter output is achieved by raising the switching frequency. However in the field of high voltage and high power applications, the switching frequency of the power device has to be restricted below 1 KHz due to the increased switching losses. So the harmonic reduction by raised switching frequency of two-level inverters becomes more difficult in high power applications. From the aspect of harmonic reduction and high Dc-link voltage level, three-level approach looks like a most alternative.

2. ANALYSIS OF TWO LEVEL INVERTERS

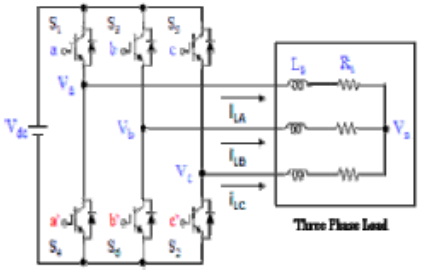

Figure.1 Three-Phase two level voltage source inverters

Space Vector Modulation (SVM) is a more sophisticated technique for generating sine wave that provides higher voltages with lower total harmonic distortion. The circuit model of a typical three-phase two level voltage source PWM inverter is shown in "Figure.1". S_1 to S_6 are the six power switches [2] that shape the output. When an upper transistor is switched on, i.e. when a, b or c is 1 and the corresponding lower transistor is switched on, i.e. the corresponding a', b' or c' is zero. Therefore, the on and off states of the transistors can be used to determine the output voltage. If two switches, one upper and one lower switch conduct at the same time such that the output voltage is $\pm V_s$, the switch state is 1.If these two switches are off at the same time, the switch state is 0.

A .SWITCHING STATES

The total number of switching states in an "N" level inverter is "$N^{3"}$. So the total number of switching states in a "2" level inverter is "$2^{3"}$ that is

8 switching states. . They are S_0, S_1, S_2, S_3, S_4, S_5, S_6, and S_7. S_0 and S_7 are called as zero switching states because during which there is no power flow from source to load.S_1 to S_6 are called as active switching states.

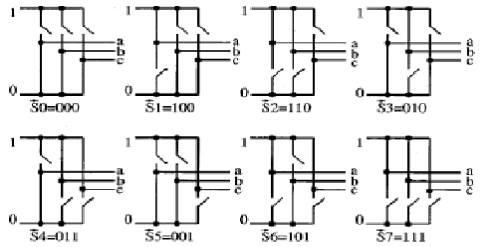

Figure.2 Switching states of two level inverters [5]

B .SPACE VECTOR DIAGRAM

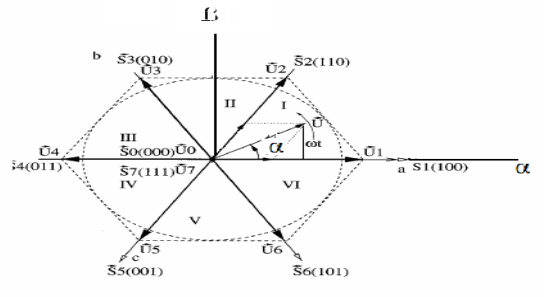

Figure.3 Space vector diagram of two level inverters [5]

Space vector diagram is divided into six sectors. The duration of each sector is 60^0. V_1, V_2, V_3, V_4, V_5, V_6 are active voltage vectors and V_0 & V_7 are zero voltage vectors. Zero vectors are placed at origin. The lengths of vectors V_1 to V_6 are unity and lengths of V_0 and V_7 are zero. The space vector V_s constituted by the pole voltage V_{ao},V_{bo} and V_{co} is defined as [3]

$V_s = V_{ao} + V_{bo}\, e^{j(2\pi/3)} + V_{co}\, e^{j(4\pi/3)}$

$V_{ao} = V_{an} + V_{no}$, $V_{bo} = V_{bn} + V_{no}$

$V_{co} = V_{cn} + V_{no}$

$V_{an} + V_{bn} + V_{cn} = 0$, $V_{no} = (V_{ao} + V_{bo} + V_{co})/3$

$V_{ab} = V_{ao} - V_{bo}$,$V_{bc} = V_{bo} - V_{co}$ & $V_{ca} = V_{co} - V_{ao}$

FOR example voltage vector V_1 that is 100

$V_{ao} = V_{dc}$,$V_{bo} = 0$ & $V_{co} = 0$

$V_{no} = (V_{dc} + 0 + 0)/3 = (V_{dc}|3)$

$V_{an} = V_{ao} - V_{no} = (2|3)\, V_{dc}$`

$V_{bn} = V_{bo} - V_{no} = = (-1|3)V_{dc}$

$V_{cn} = V_{co} - V_{no} = = (-1|3)\, V_{dc}$

$V_{ab} = V_{ao} - V_{bo} = V_{dc}$, $V_{bc} = V_{bo} - V_{co} = 0$

$V_{ca} = V_{co} - V_{ao} = -V_{dc}$

TABLE.I
SWITCHING VECTORS, PHASEVOLTAGES, OUTPUT VOLTAGES [2]

Voltage Vectors	Switching Vectors			Line to neutral voltages			Line to line voltages		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{cn}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

(Note: Respective voltages should be multiplied byV_{dc})

3. ANALYSIS OF 3 LEVEL I NVERTERS

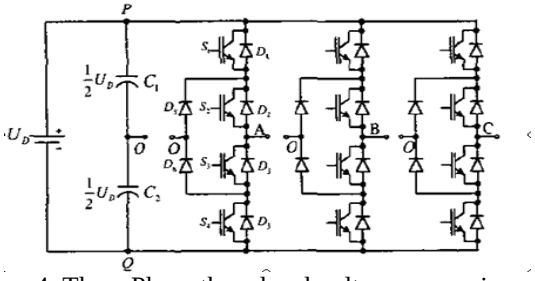

Figure.4. Three Phase three level voltage source inverters

The circuit [1] employs 12 power switching devices and 6 clamping diodes. Each arm contains four IGBTs, four anti parallel diodes and two neutral clamping diodes. And the dc bus voltage is split into three levels by two series connected bulk capacitors C_1, C_2 two capacitors have been used to divide the DC link voltage into three voltage levels, thus the name of 3-level.The middle point of the two capacitors can be defined as the neutral point 0.

TABLE.II
THE SWITCHING VARIABLES OF PHASE A [3]

V_{ao}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_a
$+V_{dc}/2$	1	1	0	0	2
0	0	1	1	0	1
$-V_{dc}/2$	0	0	1	1	0

A. SPACE VECTOR DIAGRAM

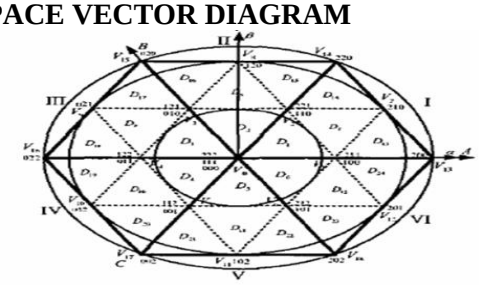

Figure.5 Space Vector Diagram of Three Level Inverters

The plane can be divided into 6 major triangular sectors (I to VI) by large voltage vectors and zero voltage vectors. Large voltage vectors are V_{13}, V_{14}, V_{15}, V_{16}, V_{17}, and V_{18}. Medium voltage vectors are V_7, V_8, V_9, V_{10}, V_{11}, and V_{12}. Small voltage vectors are V_1, V_2, V_3, V_4, V_5, and V_6. Zero voltage vectors are V_0.Phase angle α is calculated and then sector, in which the command vector V* is located, is determined as:

If α is between $0 \leq \alpha < 60°$, and V* will be in major sector I. If α is between $60° \leq \alpha < 120°$, and V* will be in major sector II. If α is between$120° \leq \alpha < 180°$, and V* will be in major sector III. If α is between $180° \leq \alpha < 240°$, and V* will be in major sector IV. If α is between $240° \leq \alpha < 300°$, and V* will be in major sector V. If α is between$300° \leq \alpha < 360°$ and V* will be in major sector VI.

B. REGION IN A PARTICULAR SECTOR

For example we are taking the space vector diagram of sector I for determining the particular region in a sector 1. Sector I contains 4 minor triangular sectors. D_1, D_7, D_{13} and D_{14} are 4 minor triangular sectors. In each of the four minor regions, the reference vector V_{ref} is located in one of the 4 regions, where each region is limited by three adjacent vectors. Then

$V_{ref} = V^* = V_x(T_x/T_s) + V_y(T_y/T_s) + V_z(T_z/T_s)$

$T_x/T_s + T_y/T_s + T_z/T_s = 1$

$T_x/T_s = \text{X}, T_y/T_s = Y \text{ and } T_z/T_s = Z$

$T_x + T_y + T_z = T_s$

Based on the principle of vector synthesis, the following equations can be written as:

X + Y + Z = 1

$V_x\text{X} + V_y\text{Y} + V_z\text{ Z} = V^*$

Modulation ratio M = $\frac{V^*}{(2|3)V_{dc}} = (3V^*|2V_{dc})$

As shown in figure.5, the boundaries of modulation ratio are Mark1, Mark 2, and Mark3 [1].

$$Mark1 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta + \sin\theta}$$

$$Mark2 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta - \sin\theta}, \theta \leq \pi/6$$

$$= \frac{\sqrt{3}/4}{\sin\theta}, \frac{\pi}{6} < \theta \leq \frac{\pi}{3}$$

$$Mark3 = \frac{\sqrt{3}}{\sqrt{3}\cos\theta + \sin\theta}$$

TABLE.III
SWITCHING STATES OF 3 LEVEL INVERTERS [1]

Switching states	S_a	S_b	S_c	Voltage Vectors
S_1	0	0	0	V_0
S_2	1	1	1	V_0
S_3	2	2	2	V_0
S_4	1	0	0	V_1
S_5	1	1	0	V_2
S_6	0	1	0	V_3
S_7	0	1	1	V_4
S_8	0	0	1	V_5
S_9	1	0	1	V_6
S_{10}	2	1	1	V_7
S_{11}	2	2	1	V_8
S_{12}	1	2	1	V_9
S_{13}	1	2	2	V_{10}
S_{14}	1	1	2	V_{11}
S_{15}	2	1	2	V_{12}
S_{16}	2	1	0	V_{13}
S_{17}	1	2	0	V_{14}
S_{18}	0	2	1	V_{15}
S_{19}	0	1	2	V_{16}
S_{20}	1	0	2	V_{17}
S_{21}	2	0	1	V_{18}
S_{22}	2	0	0	V_{19}
S_{23}	2	2	0	V_{20}
S_{24}	0	2	0	V_{21}
S_{25}	0	2	2	V_{22}
S_{a26}	0	0	2	V_{23}
S_{27}	2	0	2	V_{24}

C. SWITCHING TIME PERIOD

1) When the modulation ratio M < Mark1, then the rotating voltage vector V* will be in sector D_1 (Region 1). In a three level inverter, switching time calculation is based on the location of reference vector with in a sector. As shown in figure.5, V^* is synthesized by V_0, V_1, and V_2. In sector D_1, the length of zero voltage vector V_0 is zero & length of large voltage vector is 1.

$V^*T_s = V_1(T_1/T_s) + V_2(T_2/T_s) + V_0(T_0/T_s)$

$V_1\text{X} + V_2\text{Y} + V_0\text{ Z} = V^*$

$V^* = M(\cos\theta + j\sin\theta)$

$V_1 = 1/2, V_2 = 1/2\ (cos\,60°, +jsin\,60°) \& V_0 = 0.$

$M(\cos\theta + j\sin\theta)$=½ X + ½ (cos 60 ° + j sin 60^0) Y (1)

X + Y + Z = 1 (2)

Using (1) & (2), we can obtain X, Y & Z

$$\begin{cases} X = 2m.\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Y = m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Z = 1 - 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

2) Similarly when the modulation ratio Mark1<M< Mark2, then V^*will be in sector D_7 (Region 2).

$V^*T_s = V_1(T_1/T_s) + V_2(T_2/T_s) + V_7(T_7/T_s)$

$V_1X + V_2Y + V_7Z = V^*$ (3)

Using (3) & (2), we can obtain X, Y& Z

$$\begin{cases} X = 1 - m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Y = 1 - 2m\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Z = -1 + 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

3) Similarly When the modulation ratio Mark2 < M < Mark3 & 0 <θ <30°, then V^*will be in sector D_{13}

$V^*T_s = V_1(T_1/T_s) + V_{13}(T_{13}/T_s) + V_7(T_7/T_s)$

$V_1X + V_{13}Y + V_7Z = V^*$ (4)

Using (4) & (2), we can obtain X, Y& Z

$$\begin{cases} X = -1 + 2m\left[\cos\theta - \frac{\sin\theta}{\sqrt{3}}\right] \\ Y = m.\frac{4\sin\theta}{\sqrt{3}} \\ Z = 2 - 2m\left[\cos\theta + \frac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

4) When the modulation ratio Mark2 < M < Mark3 and 0 <θ <30°, then V^*will be in sector D_{13}

$V^*T_s = V_1(T_1/T_s) + V_{13}(T_{13}/T_s) + V_7(T_7/T_s)$

$V_1X + V_{13}Y + V_7Z = V^*$ (5)

Using (5) & (2), we can obtain X, Y& Z

$$\begin{cases} X = 2m\left[\cos\theta - \dfrac{\sin\theta}{\sqrt{3}}\right] \\ Y = -1 + m.\dfrac{4\sin\theta}{\sqrt{3}} \\ Z = 2 - 2m\left[\cos\theta + \dfrac{\sin\theta}{\sqrt{3}}\right] \end{cases}$$

4. ANALYSIS OF 3 LEVEL SPWM

The sinusoidal PWM compares a high frequency triangular carrier with three sinusoidal reference signals, knows as the modulating signals, to generate the gating signals for the inverter switches. This is basically an analog domain technique and is commonly used in power conversion with both analog and digital implementation. By comparing a sinusoidal reference signal with a triangular carrier wave of frequency, gating signals are generated. The frequency of reference signal determines the inverter output frequency and its peak amplitude controls the modulation index M and then in turn the RMS output voltage. The number of pulses per half cycle depends on the carrier frequency. Within the constraint that two transistors of the same arm cannot conduct at the same time.

Sinusoidal pulse width modulation [2] is used to control the inverter output voltage and maintains good performance to synthesize AC voltage wave forms in several applications, such as uninterruptible power supplies, motor drives and active filters.

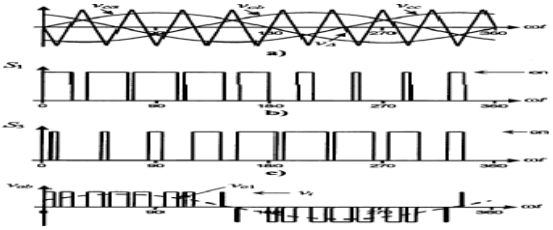

Figure .6 waveforms of SPWM

Inverter output voltage has the following features

1) PWM frequency is same as the frequency of trigging voltage V_{tri}.

2) Amplitude is controlled by the peak value of control voltage V_{cntr}.

3) Fundamental frequency is controlled by the frequency of control voltageV_{cntr}.

There are three sinusoidal reference waves (V_{ra},V_{rb},V_{rc}) each shifted by 120^0. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signals for that phase. Comparing the carrier signal (V_{cr}) with the reference phases (V_{ra}, V_{rb}, and V_{rc}) produces g_1, g_3 and g_5.

5. SIMULATION MODELS

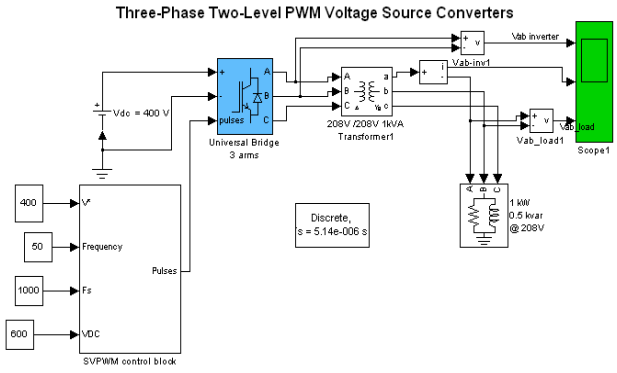

Figure .7 Simulink Model of 2- level SVPWM Inverters

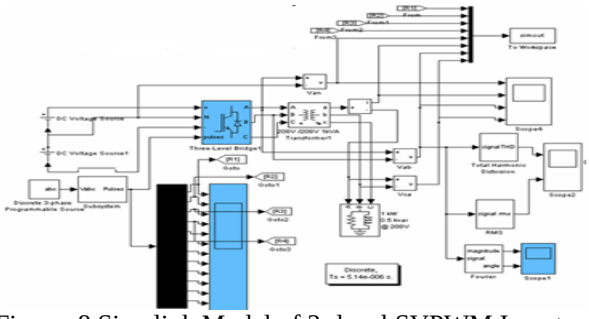

Figure .8 Simulink Model of 3- level SVPWM Inverters

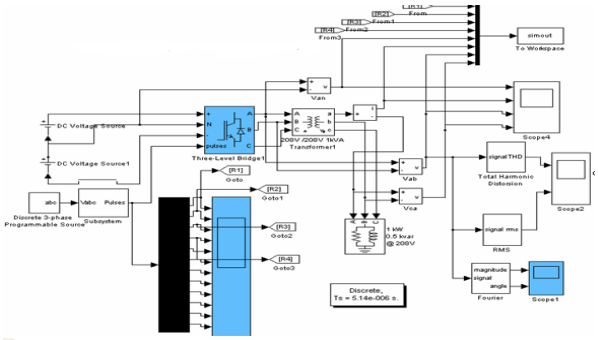

Figure.9 Simulink Model of 3- level SPWM Inverters

6. SIMULATION RESULTS

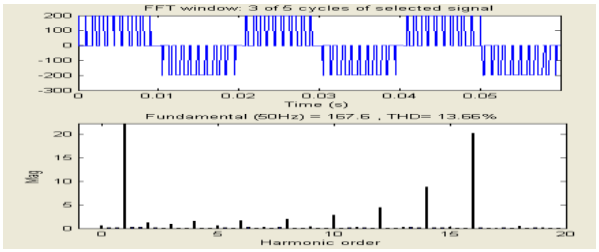

Figure.10THD of SVPWM 2 level inverter voltage

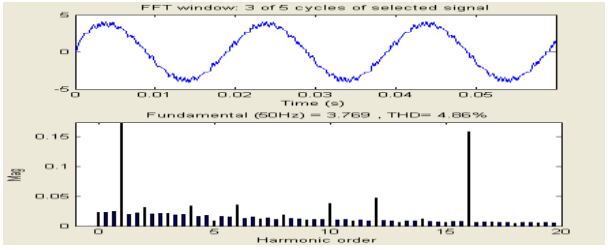

Figure.11 THD of SVPWM 2 level inverter current

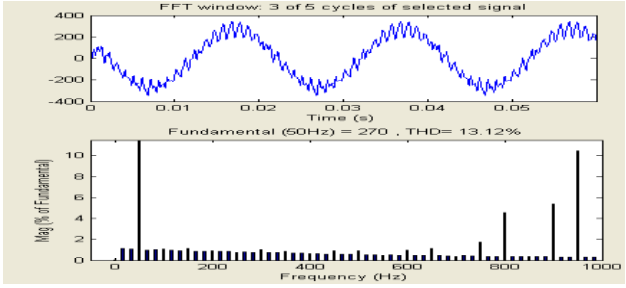

Figure.12 THD of SVPWM 2 level inverter load voltage

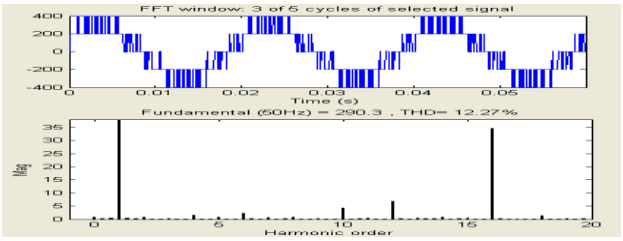

Figure.13 THD of SVPWM 3 level inverter voltages

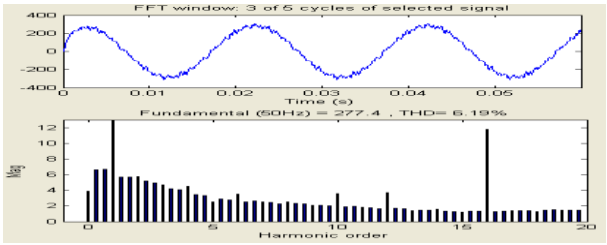

Figure.14 THD of SVPWM 3 level inverter load voltage

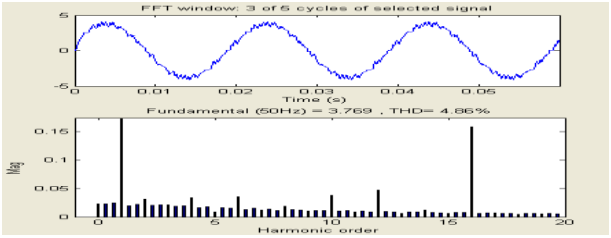

Figure.15 THD of SVPWM 3 level inverter current

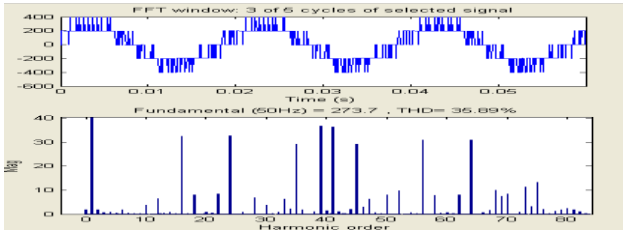

Figure.16THD of SPWM 3 level inverter line voltage

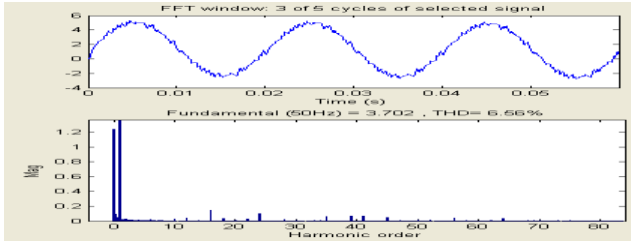

Figure.17THD of SPWM 3 level inverter current

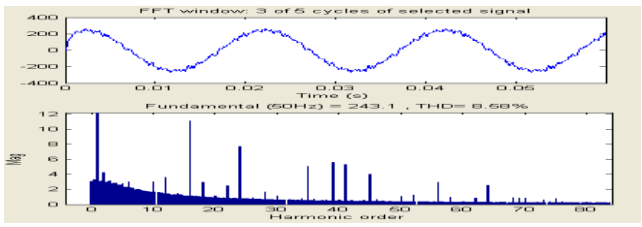

Figure.18THD of SPWM 3 level inverter load voltage

TABLE.IV

COMPARISION OF SVPWM & SPWM INVERTERS

Type	V_{ab} Inverter voltage	V_{ab} Load voltage	Inverter current
SVPWM TWO LEVEL INVERTER	38.74%	13.12%	11.80%
SVPWM THREE LEVEL INVERTER	12.27%	6.19%	4.86%
SPWM THREE LEVEL INVERTER	35.89%	8.58%	6.56%

TABLE.V

SIMULATION PARAMETERS FOR TWO LEVEL & THREE LEVEL SVPWM INVERTER

Input DC link voltage for 2 level inverter	400V
Input DC link voltage (V_{dc1}) for 3 level inverter	200V
Input DC link voltage (V_{dc2}) for 3 level inerter	200V
Input voltage for 2 & 3 level inverter	400V
Fundamental frequency (F) for 2 & 3 level inverter	50HZ
Switching frequency (F_s) for 2 & 3 level inverter	1000 HZ
Transformer for 2 & 3 level inverter	Ratio on Transformer (208/208V 1KVA)
Three phase ac RL load Active power for 2 & 3 level inverter	1kw
Three phase ac RL load Reactive power	500KVAR

6. CONCLUSION

This paper work provides successful attempt to analysis & comparison of SVPWM & SPWM inverters. In this paper, SVPWM strategy for two level & three level inverters and SPWM strategy for three level inverters is reported. From this paper SVPWM strategy concludes that, it generates less THD compared to SPWM strategy and also this paper concludes that when the number of levels increasing, harmonics are reduced for same technique as well as for different techniques. Simulation results have been given for R-L load in this paper. This software implementation used in this paper can be extended further to three phase Induction Motor load which will be a future enhancement. The proposed scheme is used for future works with high levels that is more than three level inverters.

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