AN ZIG-ZAG CONCATENATED DOUBLE RUNG H-BRIDGES BASED MULTILEVEL VOLTAGE SOURCE INVERTER STRUCTURE

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Abstract: *These instructions give this paper suggests a newer multilevel inverter (MLI) with lesser number of switches (hence gate drivers) and active devices in conduction path. The key philosophy imbibes that the structure constituted using series connected twin sourced half bridge power modules. Each power module composed of two isolated dc sources/capacitors and six switches. The proposed topology makes use of few modules with reduced number of components for a specific level of output voltage as compared to cascaded H- Bridge inverter. The proposed Zig-Zag Concatenated Double Rung H-Bridges Based MLI (ZCDRHBMLI) is thoroughly investigated in MATLAB/Simulink based simulation and the performance adequately validated through experimental results. Thus, this contribution clues the emergence of a new variety of MLI and brings a different dimension in power control applications.*

Key words: *Component reduced multilevel inverter (MLI), Zig-Zag Concatenated Double Rung H-Bridges Based MLI (ZCDRHBMLI), Pulse Width Modulation (PWM)*

1. Introduction.

For the medium and high voltage/power control, the structures to handle more voltage with smaller devices and synthesize high quality output are imperative. The power converter structures like multi-pulse rectifiers, multilevel inverters (MLIs), interleaved dc-dc converters stand in such a list. MLIs have embarked in the dc-ac conversion family as a winsome alternative in the medium-voltage energy control. Contemporary industries demands high power systems and the rating surpassed the megawatt level. Today, even the adjustable speed ac drives in the megawatt range need to be attached to the medium-voltage network. Ostensibly, it is impasse to connect the available semiconductor power switches directly to medium voltage grids. The solution this problem has already been provided by the family of MLIs, which has capability to work with higher voltage levels [1]–[2]. MLIs collude an array such switches of lower rating and capacitor voltage sources and generate output voltages of stepped fashion. The working combination of the switches enlivens the addition of the capacitor voltages, which enable the output to reach high value, while the individual power switches require enduring only reduced voltages. Addition of more number of levels (through more capacitor/separate voltage sources) will urge the output voltage with more steps and it will result in reduced harmonic distortion. Eventually, a distortion free (pure sinusoidal) output wave can be achieved by an infinite number of levels. Conversely, a high number of levels augments the control intricacy and brings in voltage imbalance problems. The number of the doable voltage levels is fairly restricted not only because of voltage unbalance issues but also due to voltage clamping requirement, gating pulse segregation, circuit layout and packing constraints.

There has been an incessant effort to device topologies with reduced component count and also to have topology specific pulse width modulation (PWM) strategies. There are different circuit arrangements (topologies) to achieve a specific number of levels of output. Three different basic topologies of MLI have been proposed, initially, and being used in various applications: diode-clamped (neutral-clamped) [3]; capacitor- clamped (flying capacitors) [1], [4]; and cascaded H-bridge (CHB) with separate dc sources (SDCs) [1], [5]. The field applications comprise use in laminators, mills, conveyors, pumps, fans, blowers, compressors, static VAR compensators, photovoltaic systems and so on [6-11]. The first work on the CHB was materialized in 1975 with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage [12]. By exploiting the CHB inverter, with diodes blocking the sources, the diode-clamped MLI was then originated; the circuit topology succeeded in the 1980s. Later, a category of MLIs based on a multilevel dc link (MLDCL) and a basic H-bridge inverter has been proposed to eliminate roughly half the number of switches, their gate drivers, clamping diodes, and capacitors by Gui-Jia Su [13]. This MLDCL has enjoyed the options with the diode-clamped phase leg, flying capacitor phase leg and cascaded half bridge cells.

A MLI topology founded on a H-bridge structure with four switches united to the dc-link has been archived [14]. The required pulse width modulation (PWM) has been devised from the sun-harmonic PWM (SHPWM) method. Using the basic principle of the variant of SHPWM, POD (phase opposition disposition) modulation method, a newer PWM method which necessitates only one carrier signal has been hinted. The switching sequence to

balance the capacitor voltage has also been deemed. The primary aim of the proposed topology is minimizing the number of components used and hence the size, require number of gate drivers etc. A host of multilevel (ML) converters based on the ML clamping principle has been introduced. With this principle, a ML clamping module conveys supplementary levels for synthesizing the output waveforms of a diode-clamped MLI dc-ac power converter. The fundamental building block of the ML clamping scheme is the ML clamping cell, which is composed of a pair of dc sources associated with one single-pole/triple-throw type of switch arrangement. The number of series-connected ML-clamping cells will situate the number of levels of the synthesized waveform [15]. Three different MLDCL MLIs have been designed with basic H-bridge to wane the number of switches. The MLDCL structure can be any one amid diode clamped, flying capacitor and cascaded structures. A superior five- level modular multilevel-clamped composited multilevel converter (5L-M-MC^2) has been devised to retract the total harmonic distortion (THD) of the line-to-line voltage and to a bridge the circuit structure [16].

In this paper, a new MLI with reduced number of switches, gate driver units and devices in conduction path is proposed. The key philosophy imbibes that the structure constituted using series connected twin sourced half bridge power modules. Each power module composed of two isolated dc sources/capacitors and six switches. The proposed, Zig-Zag Concatenated Double Rung H-Bridges Based MLI (ZCDRHBMLI), topology makes use of few modules with reduced number of components for a specific level of output voltage as compared to CHB inverter.

2. Proposed ZCDRHBMLI Topology

The generalized structure of the proposed ZCDRHBMLI is pictured in Fig.1, which is constructed using series connection of several twin sourced half bridge power modules. Each power module in this topology includes six power switches, two lesser than the usual cascaded H-bridge MLI with eight power switches that radically reduces the power circuit intricacy and simplifies modulator circuit design and accomplishment. The proposed topology utilizes 'n' number of voltage sources (V_1, V_2...V_n) and the (n+3) number of switches (S_1, S_2...S_{n+2}, S_{n+3}) which are complementary to the switches (S_1', S_2'...S_{n+2}', S_{n+3}') in order to avoid interlooping problems. This topology is modular and can be increased to produce higher levels by connecting 'k' modules, where 'k' is the

number of modules. The topology is free from voltage balancing problems due to isolated voltage sources. Each power module is capable of producing five level (+2V_{dc}, +V_{dc}, 0, -V_{dc}, -2V_{dc}) in the output voltage. Figs. 2 to 5 depict the operating modes to extract different levels of output voltage. As seen from Figs. 2 and 4, the switches (S_1, S_2', S_4, S_6', S_7') and (S_1, S_3', S_4', S_5', S_7) are turned on to produce +V_{dc} and +3V_{dc} in the nine level inverter. The relation between power modules (k) and number of dc sources (n) is given by n= (2×k). The number of levels (m) appeared in the output voltage, number of switching devices and devices in the conduction path are [(4×k)+1], [(6×k)+2] and [(2×k)+1] respectively. The details in Table 1 establish the number of power components entailed between the proposed and conventional topologies.
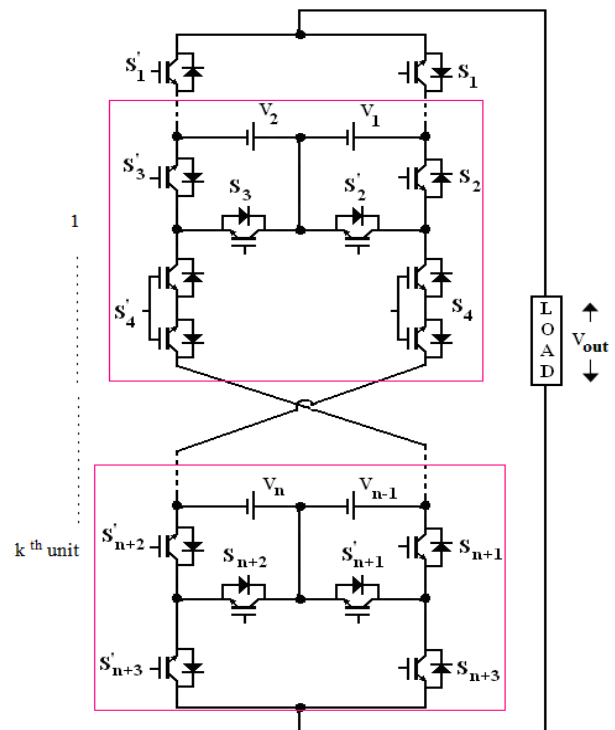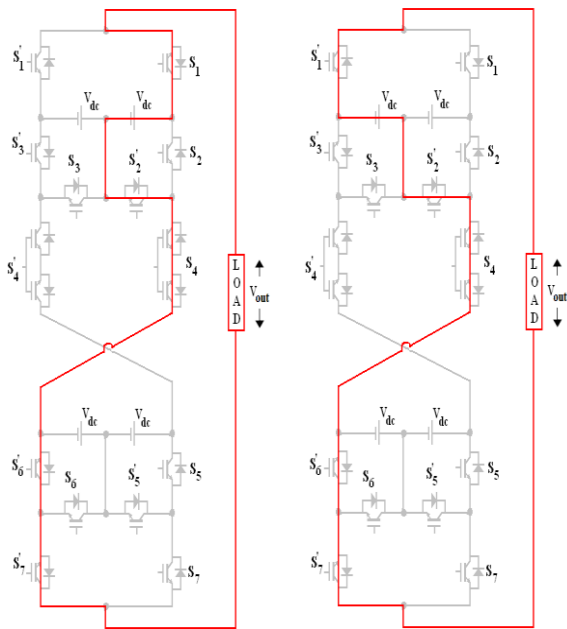

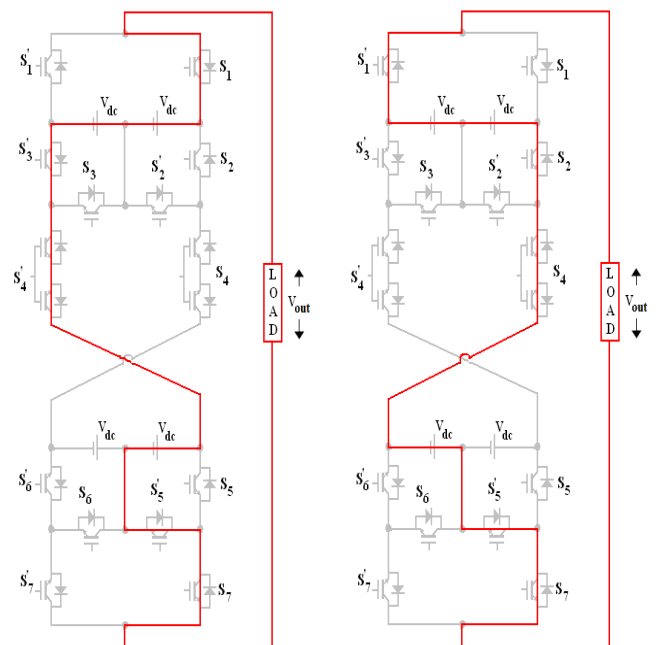Fig. 1 Proposed Topology

Fig. 2 Operating mode- ($\pm V_{dc}$)

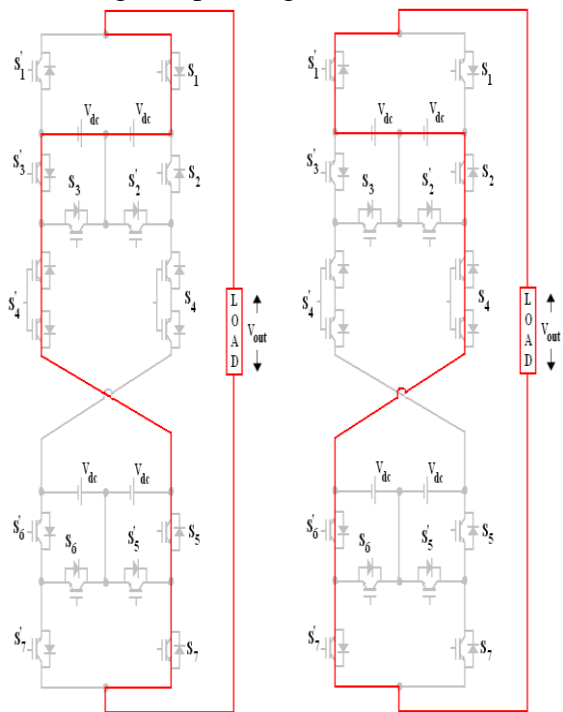Fig. 4 Operating mode- ($\pm 3V_{dc}$)

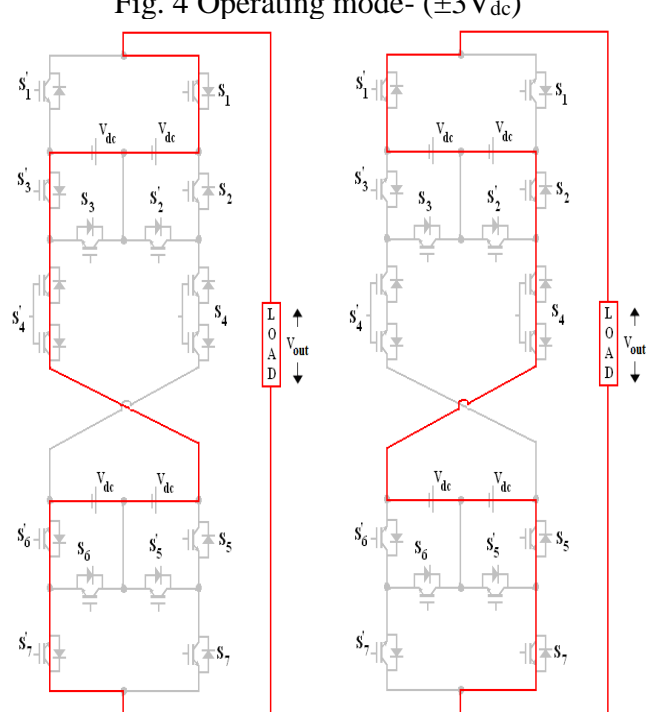Fig. 3 Operating mode- ($\pm 2V_{dc}$)

Fig. 5 Operating mode- ($\pm 4V_{dc}$)

Table 1 Component Comparison of various MLI Topologies

Topology	Main switches	Main diodes	Gate drivers	Clamping diodes	Flying capacitors	Dc-link capacitors	Total Component Count
CHBMLI	2(m-1)	2(m-1)	2(m-1)	-	-	(m-1)2	13(m-1)/2
Diode clamped	2(m-1)	2(m-1)	2(m-1)	2(m-3)	-	(m-1/)2	(17m-25)/2
Capacitor clamped	2(m-1)	2(m-1)	2(m-1)	-	(m-3)	(m-1/)2	(15m-19)/2
Cascaded Half- Bridge MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	-	-	(m-1)2	(7(m-1)+24)/2
Diode Clamped MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	(m-3)	-	(m-1/)2	9(m+1)/2
Capacitor Clamped MLDCLI	(m-1)+4	(m-1)+4	(m-1)+4	-	(m-3)/2	(m-1/)2	(8m+14)/2
SPSMLDCLI	(3m-1)/2	(3m-1)/2	(3m-1)/2	1	-	(m-1/)2	(5m-1)
Proposed	(3m+1)/2	(3m+1)/2	3(m-1)/2	-	-	(m-1/)2	(5m-1)

3. PWM Strategy

The proposed topology is designed to produce Nine levels in the output voltage using well known sub-harmonic PWM strategy. For 'm' level proposed MLI, (m-1) triangular carriers of the same amplitude and frequency, are transposed vertically in phase or out of phase or 180° phase shifted between the carrier signals with each other. The PWM signals required to switch the devices are obtained from direct comparison between the triangular carriers (V_{cr1}, V_{cr2}, V_{cr3} and V_{cr4}) and the modulating reference sine signal ($M \times \sin wt$) as depicted in Fig. 6. 'M' is the modulation index. Fig.7 illustrates the analog circuitry for implementing the PD(phase Disposition)-PWM for the Nine level output.
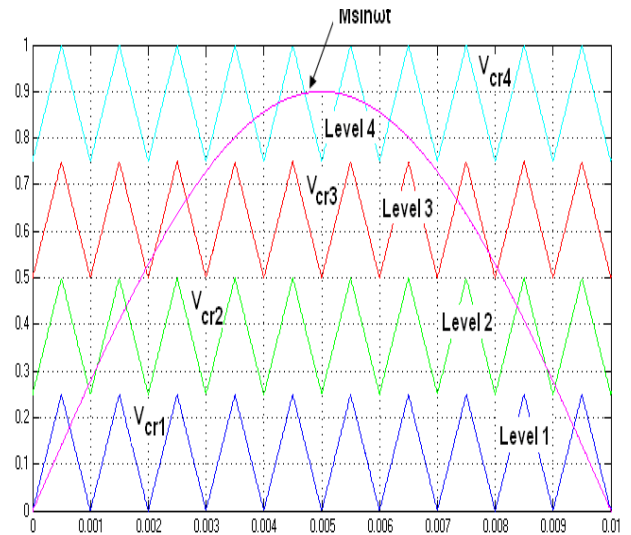

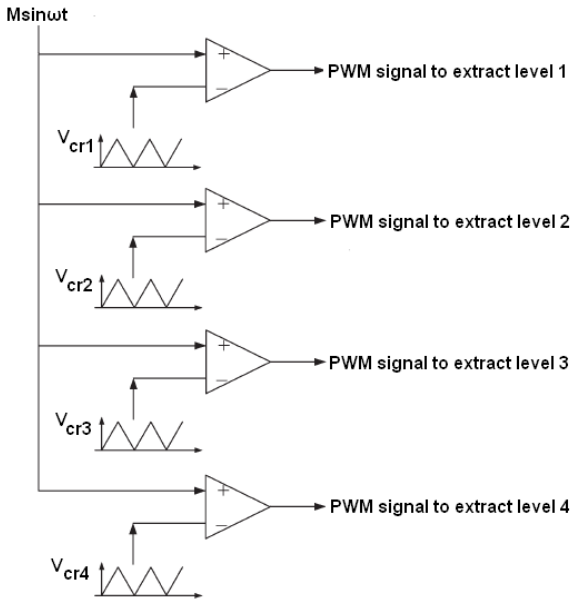Fig. 6 Phase Disposition-PWM technique

Fig. 7 PD-PWM scheme for single phase

Nine level Inverter

4. Simulation Results

For simulation, MATLAB-Simulink R2010a software is used. The simulation parameters are: $V_1=V_2=V_3=V_4=V_{dc}=75V$ each and the switching frequency is 2kHz. AnInductive load is considered with values, R= 150Ω and L= 100mH. The Fig. 8 and Fig. 9 depict the output voltage waveform and its harmonic spectrum respectively for M=1. The inductive load current for the single phase Nine level Inverter is portrayed in Fig.10, and it traces a near sinusoidal shape due to the filtering action of the inductive load and the supportive carrier frequency. The representative gate pulses are depicted in Fig. 11 and Fig. 12.
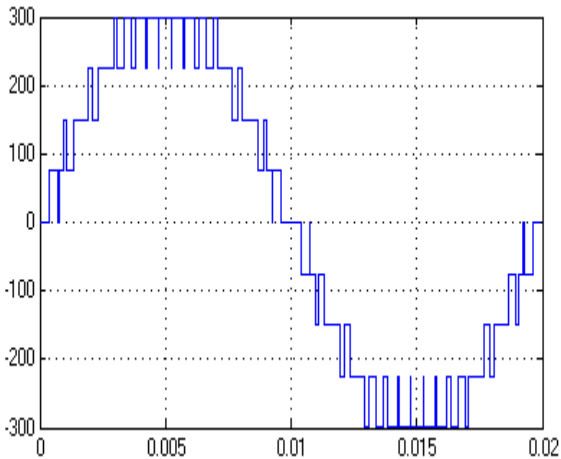

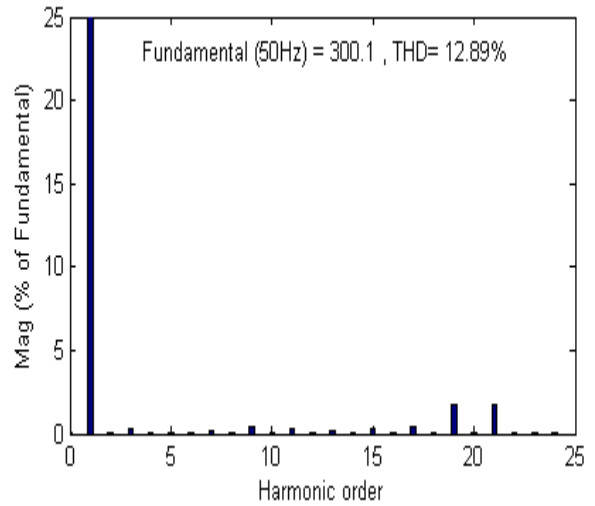
Fig. 8 Output voltage waveform
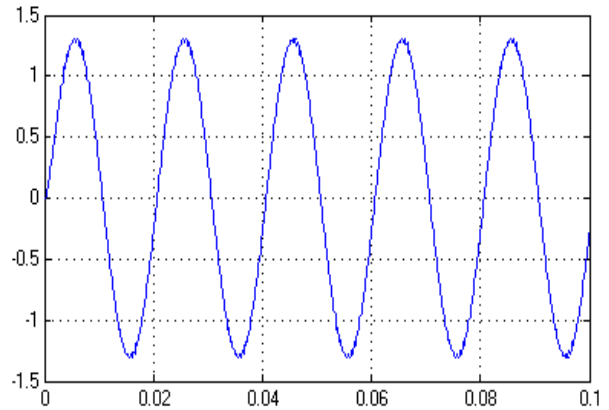

Fig. 9 Output voltage Spectrum
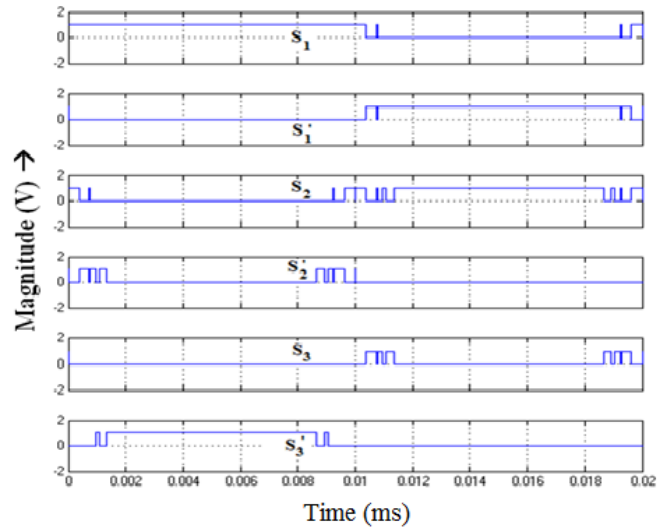

Fig. 10 Load current wave form

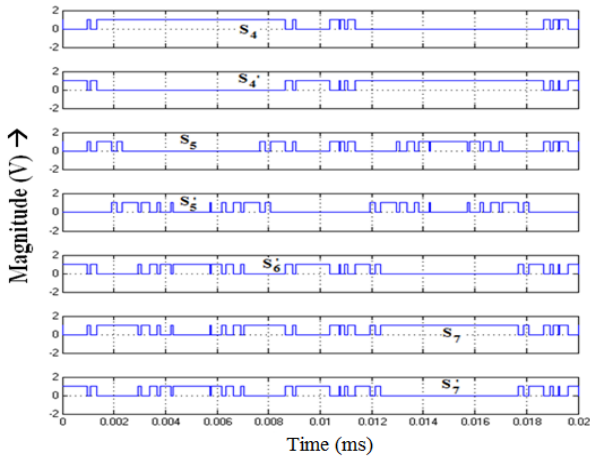Fig. 11 Representative gate pulses of upper module-ZCDRHBMLI

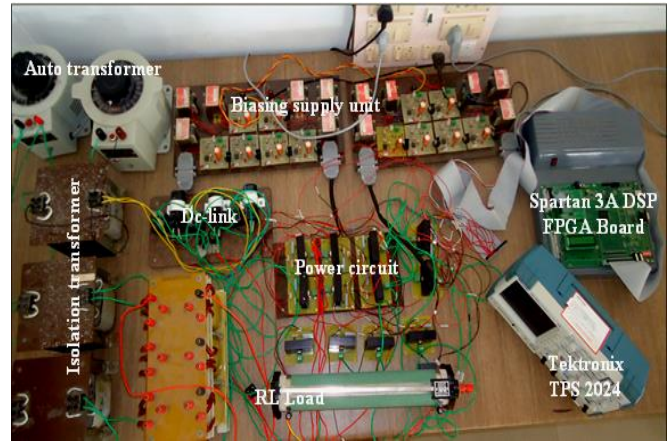Fig.12 Representative gate pulses of lower module- ZCDRHBMLI

Fig. 13 Prototype of proposed single phase Nine level Inverter

5. Experimental Results

The experimental prototype for the proposed topology depicted in Fig.13 is constituted using the power IGBT, BUP306D and tested for the same load specifications (used in simulation study) to validate the simulated performance. The PD-PWM is implemented in Xilinx Spartan 3E-500 FG320 FPGA board. The PD-PWM architecture is designed using the VHDL language. The functional simulation of the architecture is carried out using the tool Modelsim 6.3. The Xilinx ISE 13.2 synthesize tool is employed for the Register Transfer Level (RTL) verification and implementation. Then, the designed architecture is configured to the Xilinx Spartan 3E-500 FG320 FPGA device. The output voltage waveform, the harmonic spectrum and the load current waveform for nine levels output for similar specifications are shown in Fig.14, Fig.15 and Fig.16 respectively. The experimental results arbitrate in par with the simulation results and highlight the practical applicability of the proposed MLI topology. Table 2 compares the key results of experimentation with the simulation. A close imitation of results in the hardware is evidenced. Subtle remission in the fundamental component is due to the forward device drops, which have not been included in the system level software (MATLAB)-based simulation study. Fig.17 demonstrates the number of devices in the conduction path.
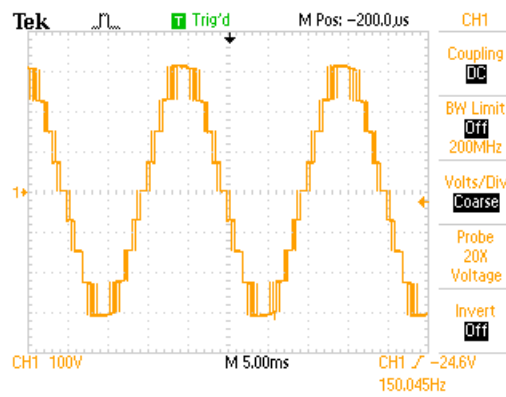

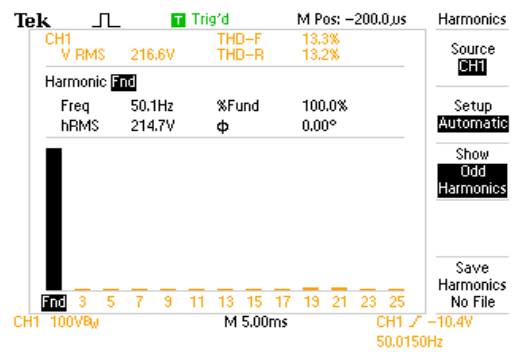Fig. 14 Experimental output voltage waveform

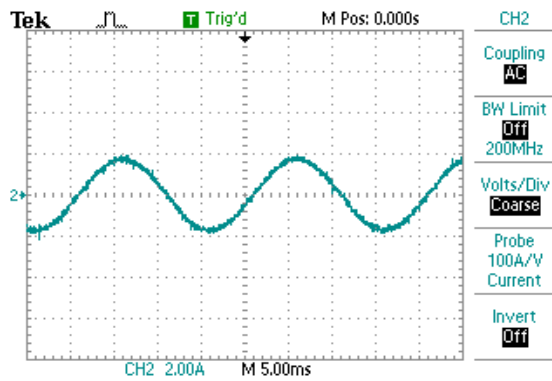Fig. 15 Experimental output voltage harmonic spectrum

Fig. 16 Inductive load current waveform

Table. 2 Comparisons of Simulation and Experimental Results

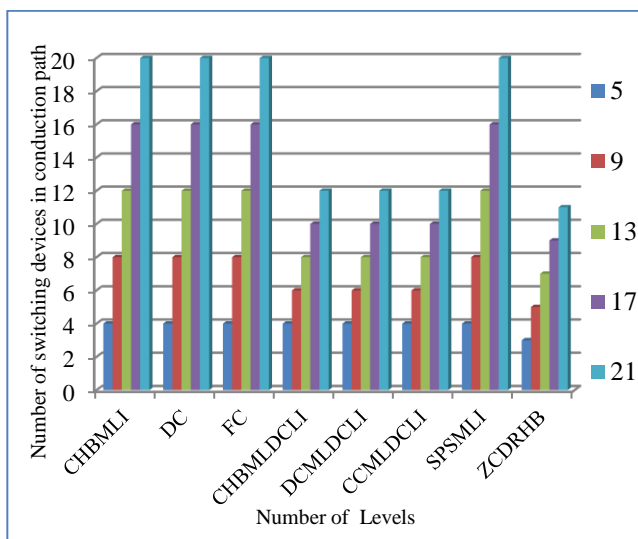| M	V_1		THD	
	Simulation	Experimental	Simulation	Experimental
0.5	106.1	105.0	26.67	28.12
0.6	127.3	125.9	24.22	25.12
0.7	148.3	146.4	21.07	24.00
0.8	169.6	167.1	16.90	17.20
0.9	190.9	188.9	16.76	17.91
1	212.6	211.1	13.45	15.24

Fig.17 Number of switching devices in conduction for different output levels

6. Conclusion

A new reduced component MLI using dual isolated voltage sources configured in half bridge structure has been developed. The topology has been extended for higher levels with relatively lesser number of power components compared with existing MLI topologies. The proposed topology has been restructured in asymmetrical configuration to pull out the desired number of voltage levels from the same number of voltage sources and bring out a higher quality output voltage spectrum. The consistent number of switches in each conduction sequence has been dragged to minimize conduction losses and hence, better efficiency. The MATLAB based simulation and the Xilinx Spartan 3E-500 FG320 FPGA supported testing results have also been provided to suit the proposed topology for renewable energy and solid state drive applications.

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