A SITO DC-DC CONVERTER HYBRID CASCADED MULTILEVEL INVERTER TOPOLOGY FOR STAND-ALONE PV APPLICATIONS

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Abstract: *The Photovoltaic (PV) is an unavoidable segment in renewable energy based power generation system. The two stage power conversion is a best pay tribute to stone alone such as EV charging station or grid-connected PV power system Nevertheless, the power converters design and control integration must be prized in order to achieve the efficiency and reliability. In this paper, a new single input triple output non-isolated DC-DC boost converter (SITO DC-DC converter) and a 15 level reduced switch hybrid H-bridge multi-level inverter (MLI) are designed for a stand-alone PV system which is most suitable to both domestic and industrial applications. To interface the DC - DC converter and DC-AC converter, a new hybrid pulse width modulation technique (PWM) is proposed which reduces the total harmonic distortion (THD) of the output voltage and mainly SITO converter reduces the voltage balancing problem in MLI while converting DC to AC. The proposed system is simulated using MATLAB/Simulink system software and laboratory scale setup is build and implemented by using SPARTAN 3 DSP controller. The simulation and experimental results are confirmed proposed converters reward.*

Index Terms: *SITO DC –DC converter, cascaded H-bridge MLI, Pulse Width Modulation (PWM) technique, total harmonic distortion (THD), SPARTAN 3 DSP controllers.*

1. Introduction

Usage and demand of renewable energy sources (RES) is increasing day by day in order to reduce the dependency on conversional energy source which plays a major role in the climatic change. Among the various RES, more research and more focus is turned towards photovoltaic (PV) system because of reliability, less impact on environment and cost factor involved in the energy production process. Standalone PV system such as EV charging station and other industrial application is been encouraged in all the countries. Energy conversion process involved in standalone PV system is mainly depended on converters which includes DC to DC and DC to AC. Obviously, designing appropriate PWM technique for the proposed DC to AC converters in order to reduce the harmonics of the output is being a big challenge.

Zeng, and Huafang Guo designed a nine level inverter with less switching devices and voltage sources [1]. It is achieved by connecting the two capacitors and a voltage source in series and parallel. Rasoul Shalchi Alishah, Seyed Hossein Hosseini, Ebrahim Babaei, and Mehran Sabahi proposed an optimized laddering technique is incorporated to design cascaded MLI structure [2] in which a new optimized pulse width modulation technique is proposed to improve the number of levels with less switching devices and DC sources. Amir Taghvaie, Jafar Adabi, and Mohammad Rezanejad introduced a new circuit topology of step-up MLI with a single DC source [3]. In that topology, by controlling the charging and discharging of switched capacitors in predetermined time, the number of levels in the output voltage is obtained. Amin Gholizad and Murtaza Farsadi proposed a improved staircase modulation for MLI [4] in which a solution for SOC for storage cells is examined. Reduced switch MLI topologies are proposed in which DC sources are connected in series and parallel [5-7] (MLISPC) and a circuit which consists of four diodes and a switch replaces the series and parallel combination of switches [8] in the MLISPC. For the same level of output voltage, only two voltage sources are needed in [8]. The proposed MLI topologies in [9-14] can be used for the PV systems application like electric hybrid vehicles etc. In all the above literatures, switching devices used to construct MLI is large and the THD value is also somewhat high. Hamed Nadeni and Ralando Burgos proposed a new circuit topology of modular multilevel converter (MMC) for photovoltaic system [15,29] in which two arm inductors are replaced with the transformer in order to reduce the circulating current and provides 50% reduction in voltage rating of power devices and capacitor size in comparison with basic MMC topology.

Irfan Ahmed proposed a simplified space vector modulation technique for MLI [16]. Emad Samadaei proposed a new E-type module for asymmetrical MLI with four unequal DC source and 10 switches to produce 13voltage levels [17]. And SHE-PWM technique has been used here to achieve high quality output voltage with lower harmonics. Jalal Amini made a general control strategy for multilevel converters (MLC) based on Knapsack problem [18] in which he has given the methods to choose appropriate control strategies for MLI. Viju Nair proposed a new method to generate more number of levels in the voltage waveform by stacking MLC [19] with lower voltage space vector structures thereby he reduced the rating of switching devices.

Elyas Zamiri proposed a new switched capacitor MLI which generates a great number of output voltage levels with optimum number of components for both symmetric and asymmetric type of DC voltage sources [20]. This is having the ability of boosting and charging of capacitors as self-balancing using binary asymmetrical algorithm. Arun Rahul proposed a closed loop capacitor voltage control strategy for cascaded MLI topologies which is fed with single DC supply [21]. Raghavendra Reddy Karasani proposed a 3-phase hybrid cascaded modular MLI topology with reduced number of switching devices for solar energy conversion system [22] in which transformer-less operation improves the quality of the output power. Ahmed Salem propose a new three phase modular MLI in which the output voltage levels can be increased by adding additional cells without increasing voltage stresses across power switches [23]. For this operation, both sinusoidal and staircase PWM have been used.

KehuYhang and Chi Zhang have done an experiment on 13level cascaded H-bridge converter in which they developed an unified selective harmonic elimination approach [24] and they formulated 3 different switching patterns and they applied these patterns on 13level inverter. Soek Min Kim designed a modified left shift PWM for inverters [25] which is for open and short circuits device faults. VenuSonti and Sachin Jain proposed a new pulse width modulation with reduced number of carrier waveforms for five level cascaded MLI to reduce the leakage current of PV array [26], electromagnetic inference and filter requirement without adding any extra switches. MaharanQuraan evaluated the performance of modular MLC with integrated battery cells used as traction drives for battery electric vehicles [27]. Mohamed Trabelsi designed a finite control set model predictive control for grid-tied packed U-cells MLI [28] with reduced of passive and active components in which he achieved low THD value in the output voltage level while balancing the capacitor voltages [31].

In this paper, a 15level hybrid cascaded MLI is designed with 10 switching devices and to reduce the voltage balancing problem, a new SITO DC-DC converter is designed for PV system application. In this proposed system, a PV array is designed and the output from PV system is fed to 15level MLI through SITO DC-DC converter which is simulated using MATLAB/SIMULINK and the results are presented here.

2. Proposed Hybrid Multilevel Inverter with SITO DC-DC Boost Converter and PV System

Fig. 1 shows the block diagram of proposed system. In which the output of solar panel is given to SITO DC-DC converter. Then the boosted and splitted output voltage from SITO DC-DC converter is given to 15level inverter to drive the RL load.

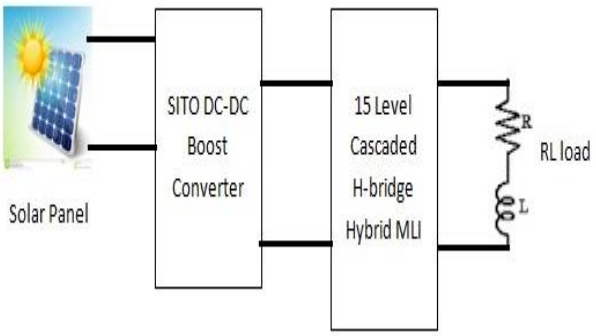

Fig 1. Block diagram of proposed system

The proposed system includes SITO DC-DC converter in order to reduce the voltage balancing problem which arises in conventional MLI. The proposed hybrid cascaded MLI generates 15levels of output voltage which can be used to drive the induction motor in industrial applications.

A. Photovoltaic Array Design

Fig. 2 shows the equivalent circuit of a solar cell. PV panel is designed for specific rating by using the following equations.

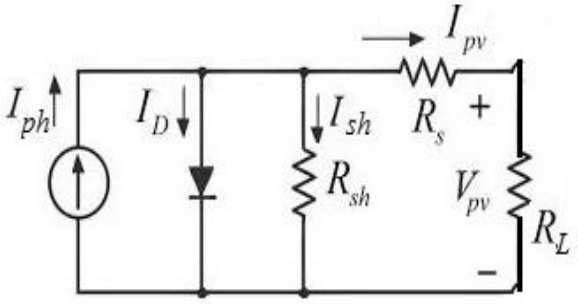

Fig 2. Equivalent circuit of a solar cell

$$I_{ph} = \left[I_{sc} + k_i \left(T_c - T_{ref} \right) \right] \left(\frac{S}{1000} \right) \quad (1)$$

$$I_{rs} = \frac{I_{sc}}{\left[\exp\left(\frac{qV_{oc}}{N_s KAT_c} \right) - 1 \right]} \quad (2)$$

$$I_s = I_{rs} \left(\frac{T_c}{T_{ref}} \right)^3 \left[\exp\left(\frac{qE_g \left(\frac{1}{T_{ref}} - \frac{1}{T_c} \right)}{KA} \right) \right] \quad (3)$$

$$I_{pv} = N_p I_{ph} - N_p I_s \left[\exp\left(\frac{q\left(V_{pv} + I_{pv} R_s \right)}{N_s AKT_c} \right) - 1 \right] - \left(\frac{V_{pv} + I_{pv} R_s}{R_{sh}} \right) \quad (4)$$

The following considerations have been made to design the PV panel in order to get 70V and 2A as output from the 210Watts PV panel which is shown in table I.

Table 1 Parameters Considered for PV System Design

S.No	Parameters	Ratings
1	I_{sc}(Short circuit current)	2.916A
2	V_{oc}(Open circuit voltage)	72V
3	T_{op}(Operating Temperature)	25^{o}C
4	T_c(Critical Temperature)	(273+T_{op}) in Kelvin
5	T_{ref}(Reference Temperature)	(273+25) in Kelvin
6	q(electron charge)	1.602*10^{-19} C
7	K(Boltzmann Constant)	1.3805*10^{-23} J/K
8	A(Ideality Factor)	1.6
9	k_i(Temperature Coefficient)	0.065 A/^{o}C
10	S(Solar radiation)	1000 W/m^2
11	E_g(Forbidden energy gap)	1.1 eV
12	N_s(number of solar cells connected in series)	216
13	N_p(number of solar cells connected in parallel)	1
14	R_s(Source resistance)	0.0002 ohms
15	R_{sh}(shunt resistance)	100000 ohms
16	V_{pv}(Ramp Maximum Voltage)	70V

B. Proposed SITO DC-DC Boost Converter

Usually in conventional methods, the output from the solar panel has to be boosted up by using a boost converter and the boosted voltage is fed to the MLI where splitting capacitors are used to split up the voltage depending on the number of output voltage levels and the scheme of the DC source (asymmetric or symmetric scheme). The usage of capacitors is given by,

$$\text{Number of capacitors, } C = 2^n + 1 \quad (5)$$

where n=number of output voltage levels of MLI.

Due to this splitting capacitors, voltage balancing problems are occurring during the splitting of voltages. Thereby, it affects the THD value of the output voltage and it creates voltage stress on the switches.

In order to rectify this problem, SITO DC-DC converter is proposed which is shown in fig.3 in this paper. By using SITO DC-DC boost converter it is able to generate three output levels which may be an asymmetric or symmetric voltage sources. In this paper, the output voltage of SITO DC-DC boost converter is (94V X 3) = 282V (i.e. 94V is a single output voltage).Boosting and splitting of voltage levels is done in this SITO DC –DC boost converter. Thereby, the THD value and voltage stress on the switching devices are reduced.

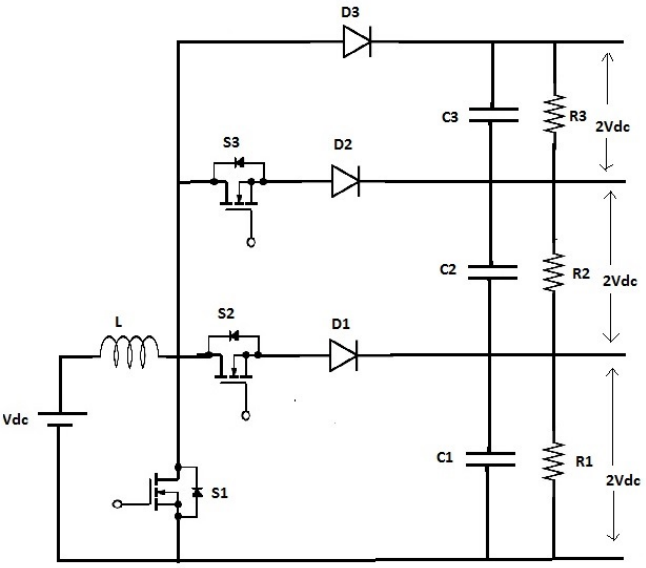

Fig 3. Circuit diagram of SITO DC-DC boost converter

C. Proposed Hybrid 15level Cascaded MLI

Number In conventional method of symmetric voltage source based MLI, 16 switching devices are needed to generate 15 level output. In this paper, a new hybrid Cascaded MLI is developed with reduced number of switching devices which is capable of generating 15 output voltage levels.

$$P = \left[\left(\frac{n-11}{4}\right)+9\right] \quad (6)$$

where n= number of output voltage levels of MLI.

To generate 15 levels of output only 10 switching devices and to generate 19 levels of output, only 11 switching devices are required.

Fig.4 shows the circuit diagram of proposed hybrid 15 level cascaded MLI. In which, there are two inverters are in cascaded connection namely upper inverter and lower inverter. Upper inverter is given with a voltage source with magnitude of V_{dc} (47V) and lower inverter is given with 3 voltage sources with magnitude of $2V_{dc}$ (94V) each (i.e total $6V_{dc}$).The upper inverter is able to produce two levels ($\pm V_{dc}$) and lower inverter produces 7 levels ($\pm 2V_{dc}, \pm 4V_{dc}, \pm 6V_{dc}, 0$). In cascaded form, the cascaded MLI produces 15 levels of output voltage with maximum voltage of 329V which is given in the equ. 9..

Number of levels given by the equation in lower inverter,

$$n_{low} = \left(2a_{low} + 1\right) \quad (7)$$

Number of levels given by the equation in upper inverter,

$$n_{upper} = \left(a_{upper} + 1\right) \quad (8)$$

where

a_{low}= Number of DC sources used in lower inverter
a_{upper}= Number of DC sources used in upper inverter
n_{low}= Number of levels produced by lower inverter
n_{upper}= Number of levels produced by lower inverter

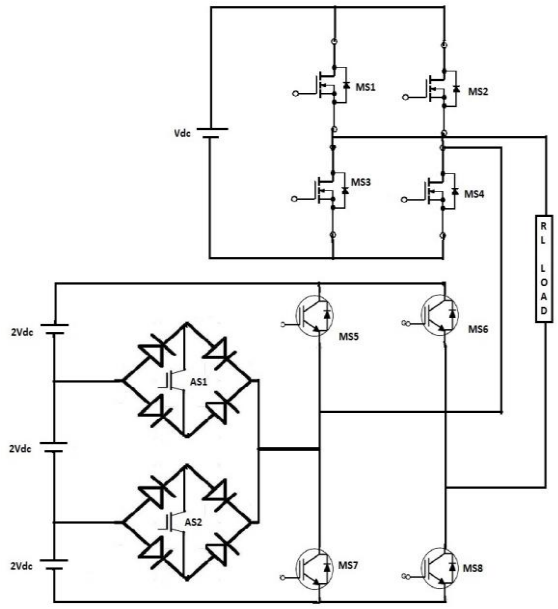

Fig 4. Circuit diagram of proposed hybrid 15level cascaded MLI converter

And maximum voltage of the cascaded MLI is

$$V_{o\max} = \left[\left(a_{upper} * V_{dc}\right) + \left(a_{low} * 2V_{dc}\right)\right] \quad (9)$$

For the proposed system in addition with SITO DC-DC boost converter, which is shown in fig.5, the number of power switching devices is given by

$$P = \left[\left(\frac{n-11}{4} + 9\right) + Q\right] \quad (10)$$

where Q= Number of switching devices in SITO converter

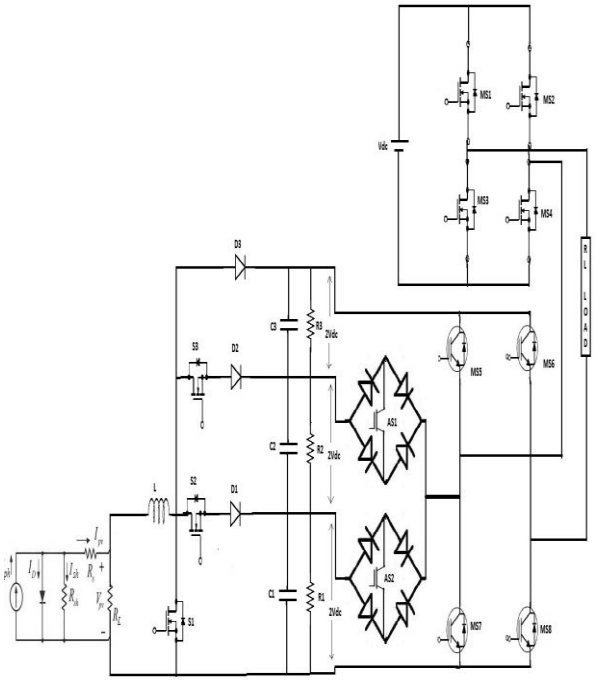

Fig 5.Circuit diagram of proposed MLI with SITO DC-DC boost converter

3. Proposed Pulse Width Modulation

A new hybrid pulse width modulation technique is proposed for this topology. Hybrid PWM technique is a combination of modified sinusoidal pulse width modulation and stair case pulse width modulation. Modified sinusoidal PWM is proposed for upper inverter to produce the output voltage at high frequency and stair case PWM is proposed for lower inverter to produce the output voltage at lower frequency. For modified sinusoidal PWM, the reference waveform is

$$V_{ref} = A\sin wt \quad (11)$$

where A is peak value of reference waveform which is given by $A = (2Q+1)$

Unified pulses

$$Z_1 = 1 \text{ if } V_{ref} > 0 \quad (12)$$

$$Z_2 = 1 \text{ if } V_{ref} < 0 \quad (13)$$

$$V_{u,\exp} = \left[round\left(\frac{V_{ref}}{0.4}\right) * 0.4 * Z_1\right] + \left[round\left(\frac{V_{ref}}{0.4}\right) * 0.4 * (-Z_1)\right] \quad (14)$$

Modified reference waveform for upper inverter is

$$V_{up,ref} = \left(V_{ref} - V_{u,\exp}\right) \quad (15)$$

By comparing modified sinusoidal reference waveform with triangular carrier waveform, switching pulses for upper inverter is to be determined which is given in table II.

For staircase PWM,

Three staircase reference waveforms R_1, R_2 and R_3 are generated along with Z_1, Z_2 where

Table 2 Switching sequence of upper inverter

Output Voltage Level	MS_1	MS_2	MS_3	MS_4
V_{dc}	1	0	0	1
0	0	0	0	0
$-V_{dc}$	0	1	1	0

$$Z_1 = 1 \text{ if } V_{ref} > 0 \quad (16)$$

$$Z_2 = 1 \text{ if } V_{ref} < 0 \quad (17)$$

The switching pulses, shown in table III, for all the switching devices including auxiliary switching devices are generated by comparing R_1,R_2,R_3 and Z_1,Z_2 which is given by the equations,

$$S_1 = \left(\overline{R_1}(or)R_3\right) * Z_1 \quad (18)$$

$$S_2 = \left[\left(R_1 * Z_2\right)(or)\left(\overline{R_1} * Z_1\right)\right] \quad (19)$$

$$S_3 = \left(\overline{R_1}(or)R_3\right) * Z_2 \quad (20)$$

$$S_4 = \left[\left(R_1 * Z_1\right)(or)\left(\overline{R_1} * Z_2\right)\right] \quad (21)$$

$$S_5 = \left[\left(R_1(xor)R_2\right) * Z_2\right](or)\left[\left(R_2(xor)R_3\right) * Z_1\right] \quad (22)$$

$$S_6 = \left[\left(R_1(xor)R_2\right) * Z_1\right](or)\left[\left(R_2(xor)R_3\right) * Z_2\right] \quad (23)$$

Table 3 Switching sequence of lower inverter

Output Voltage Level	MS_5	MS_6	MS_7	MS_8	AS_1	AS_2
2 V_{dc}	0	0	0	1	0	1
4 V_{dc}	1	0	0	1	1	1
6 V_{dc}	1	0	0	1	0	0
0	0	0	0	0	0	0
-2 V_{dc}	0	1	0	0	1	0
-4 V_{dc}	0	1	0	0	0	1
-6 V_{dc}	0	1	1	0	0	0

4. Voltage Rating of the devices

The rating of the switching devices should be selected prudently in the proposed inverter, because of the dissimilarities in the voltage rating of each device. Only one auxiliary switch is required in the proposed topology of 11-level inverter. In this case, the voltage of auxiliary switch will bounce between 0 and $2V_{dc}$ because the total voltage $4V_{dc}$ is alienated into two by splitting capacitors (i.e) $2V_{dc}$ each. Therefore, capacitor voltage of $2V_{dc}$ has to be blocked by the auxiliary switches. Likewise, two auxiliary switches are required in the proposed topology of 15-level inverter. The total voltage $6V_{dc}$ is alienated into three by three splitting capacitors (i.e) $2V_{dc}$ across each. Hence, the voltage of two auxiliary switches will bounce between 0 and 4Vdc. Further, three auxiliary switches are required in 19-level inverter. The voltages of first and last auxiliary switch will bounce between 0 and $6V_{dc}$ and the voltage of middle auxiliary switch will bounce between 0 and $4V_{dc}$. Similarly, for other levels of inverters of this topology, the voltage of first and last auxiliary switch voltage bounces between 0 and $\left((n-1)mV_{dc}/n\right)$, whereas the voltage of other auxiliary switch bounces between 0 and $\left((n-2)mV_{dc}/n\right)$, $\left((n-3)mV_{dc}/n\right)$…and so on and where n is the number of splitting capacitors and mV_{dc} is total voltage applied for the lower inverter.

5. Simulation and hardware results

Fig.6 shows the generation of pulses for upper inverter switching devices which is done by comparing the modified sinusoidal waveform with triangular carrier waveform at (400 kHz) high frequency.

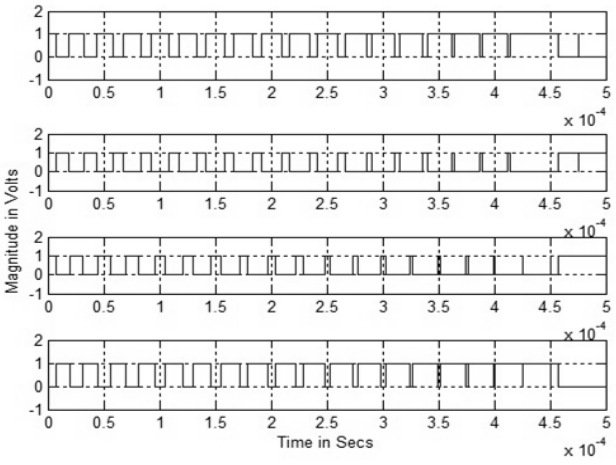

Fig 6. Gate pulse of upper inverter

Fig.7 shows the generation of pulses for lower inverter switching devices which is done by comparing the using staircase PWM with triangular carrier waveform at (50 Hz) low frequency [29].

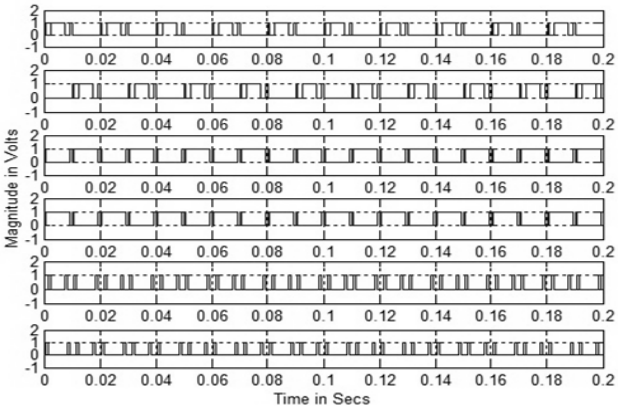

Fig 7. Gate pulse of lower inverter

Fig. 8 shows the 15level output voltage waveform of proposed MLI with voltage splitting capacitors where voltage mismatching has occurred due to voltage balancing problem.

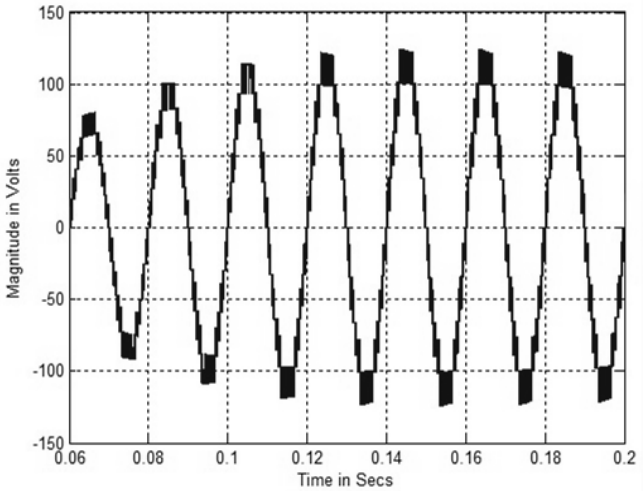

Fig 8. 15level output voltage waveform of proposed MLI with splitting capacitors

Fig. 9 shows the THD value of 15 level output voltage waveform of conventional MLI.

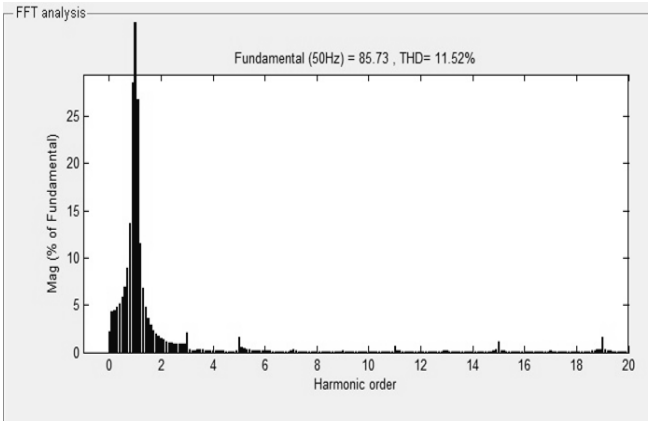

Fig 9. THD plot of output voltage of 15level proposed MLI with splitting capacitors

Fig. 10 shows the 15level output voltage waveform of proposed MLI where voltage balancing problem has overcome and in fig. 11, it is observed that the THD value of output voltage waveform of proposed MLI has been reduced when compared with conventional MLI.

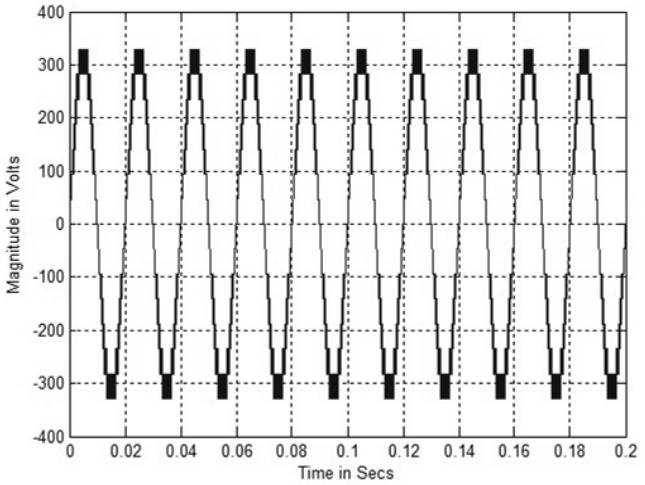

Fig 10. Output voltage waveform of 15level MLI with SITO DC-DC boost converter

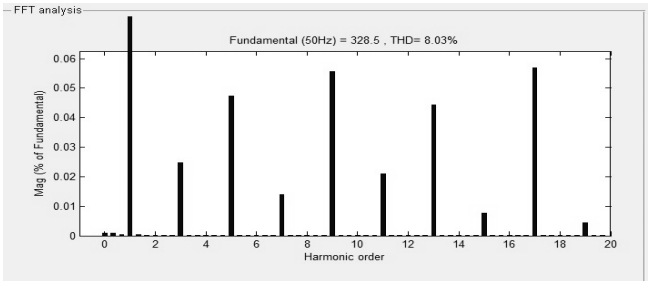

Fig. 11 THD plot of output voltage of 15level MLI with SITO DC-DC boost converter

Fig. 12.a. and 12.b. shows the hardware output of switching pulses for upper inverter.

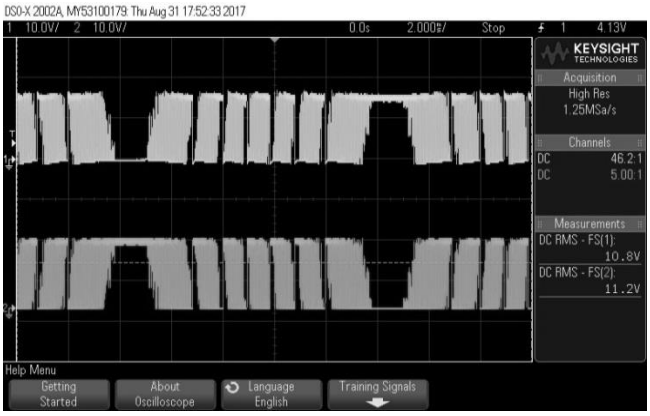

Fig 12.a. Hardware output of switching pulses for switches MS1 and MS3 of upper inverter

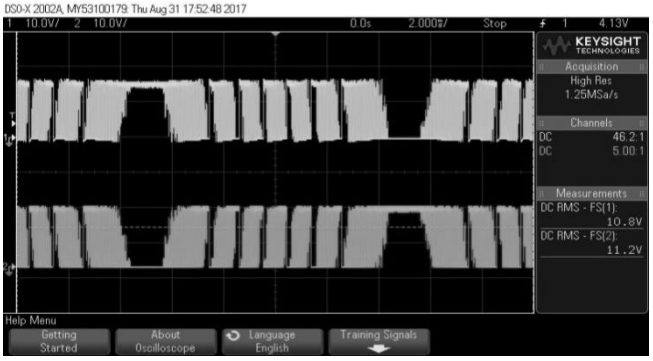

Fig 12.b. Hardware output of switching pulses for switches MS2 and MS4 of upper inverter

Fig. 13.a., 13.b. and 13.c. shows the hardware output of switching pulses for lower inverter.

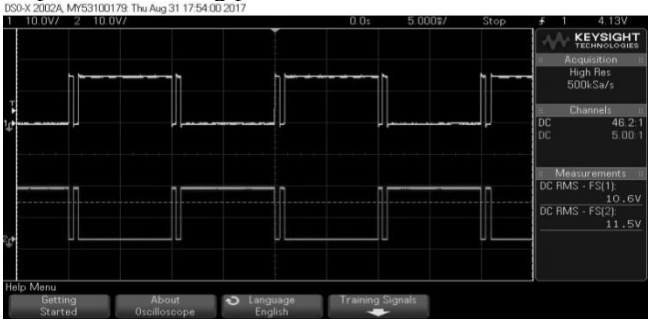

Fig 13.a. Hardware output of switching pulses for switches MS5 and MS7 of lower inverter

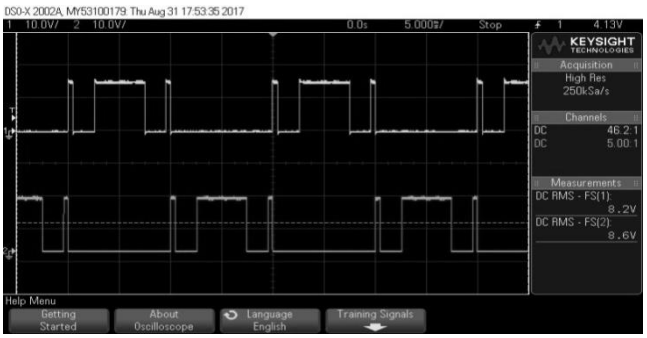

Fig 13.b. Hardware output of switching pulses for switches MS6 and MS8 of lower inverter

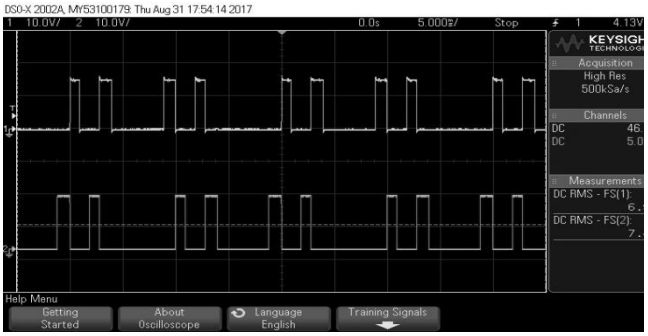

Figure 13.c. Hardware output of switching pulses for switches AS1 and AS2 of lower inverter

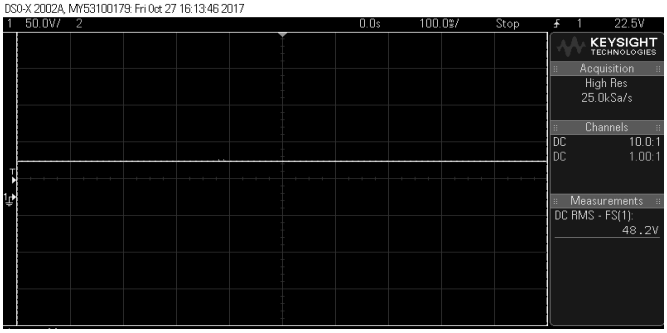

Figure 14.a. DC output voltage of boost converter given for upper inverter

Figure 14.b. DC output voltage of SITO boost converter given for lower inverter

Fig. 14.a, 14.b show the hardware output voltage of boost converter which is given as input for upper inverter and lower inverter respectively. Fig. 15, 16 shows the 15level output voltage waveform of proposed MLI with SITO boost converter that is observed from Digital storage oscilloscope and THD value of output voltage waveform respectively.

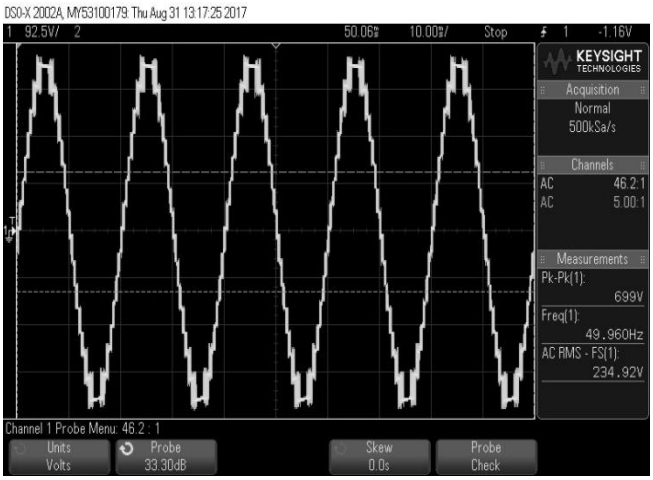

Fig 15. Output voltage waveform of 15level MLI with SITO DC-DC boost converter

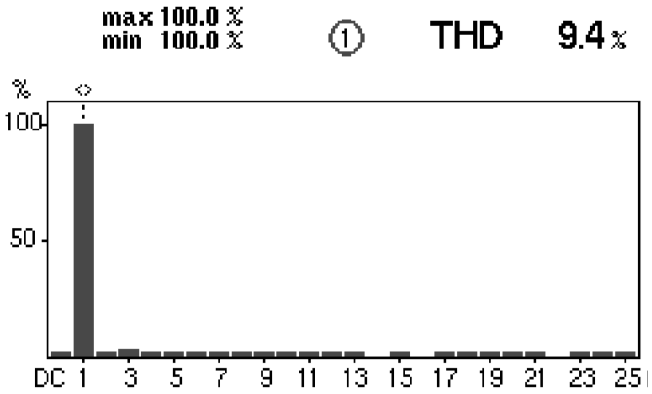

Fig 16. Output voltage waveform of 15level MLI with SITO DC-DC boost converter

Fig. 17. Hardware implementation of 15level MLI with single input triple output DC-DC boost converter

Comparison of conventional MLI [6] and proposed topology of MLI is given in the table IV and fig.18.

Table 4 Comparison of number of levels, number of switching devices, THD value and No. of DC Sources

Method	Level	No of Switch Used	THD in %		DC Sources
			Simulation	Hardware	
Type 1	15	16	11.4	16.2	1
Type 2	15	10	11.52	14.5	1
Type 3	15	10	8.02	9.4	1

In table 4,
Type 1: Conventional type MLI with single DC source and splitting capacitors
Type 2: Proposed MLI with single DC source and splitting capacitors
Type 2: Proposed MLI with single input triple output DC-DC boost converter

Table 5 Comparison of Different levels of MLI constructed by using the proposed topology

S.No	Method	Level	Number of Switching Devices Used
1	MLI with SITO boost Converter	11	9
2		15	10
3		19	11

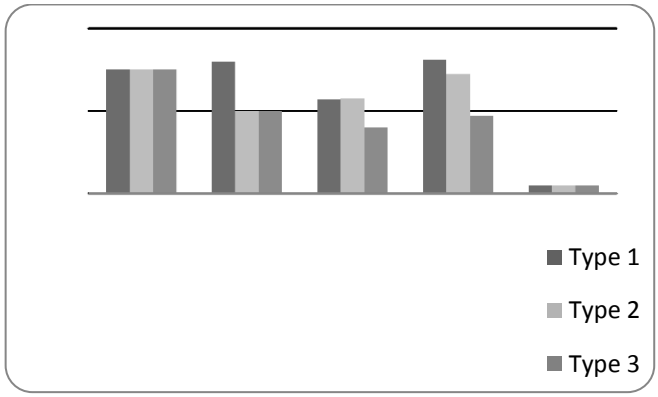

Fig 18. Graphical comparison of 15level conventional MLI with proposed topology

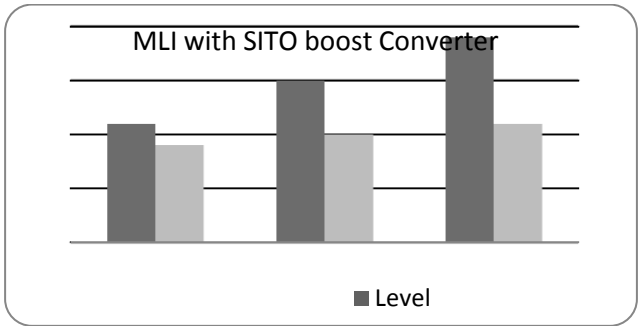

Fig 19. Graphical comparison of different levels of proposed MLI topologies

6. Results and Discussions

The results of the proposed MLI topology are compared with the conventional type of MLI topology [1], [2], [3], [5], [6], [11] and it is exhibited in the above sections. From the comparison, it is concluded that the proposed type of MLI with SITO boost converter has been found to be more efficient with low value of THD values of output voltage, free from the voltage balancing problems which cause severe troubles in the case of high voltage applications and the number of power semiconductor switching devices required for higher voltage level generations is also reduced. It is concluded that the performance of combined proposed MLI with SITO boost converter is better than the combined proposed MLI with single DC source and splitting capacitors. During Hardware implementation of the proposed SITO boost converter, a small deviation is found in the output voltage of SITO boost converter when compared with simulation output which is shown in the table 6 and fig. 20.

Table 6 Comparison of output voltage of SITO boost converter between hardware and simulation outputs.

Type	MLI with SITO boost Converter Output Voltage(in Volts)
Hardware	*99+101+101=301V
Simulation	*94+94+94=282V

*which represents the triple output voltage of SITO converter.

Fig 20. Graphical comparison of hardware and simulation output voltages of SITO converter

7. Conclusion

The cascaded 15 level hybrid SITO DC-DC boost converter is proposed with reduced number of switching devices and generates output level with low THD value when compared with conventional MLI which is shown in the table IV. The comparison table for different level of MLI which is constructed by

using the proposed topology is shown in table V and fig.19. Proposed SITO DC –DC boost converter eliminates the voltage balancing problem which is arising in conversional MLI and this is the best boost converter for solar PV application. Thus, it can be used for medium and high power applications.

8. References

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